

MODEL NAME : Warlock MLK ADL

PCB NO : DA6002E0000

PCB 2X2 HDL5A LA-L946P REV10

M/B 1 S

ADL-P+NPCX993
(UMA)
2021-09-22
REV : 1.0 (A00)

ADL CPU ES2

UC1
SA0000ERH0L
QY4Y@
S IC A31 FJ8071504661126 QY4Y Q0 1.2G S

UC1
SA0000EQC0L
QY4T@
S IC A31 FJ8071504661121 QY4T Q0 1.2G S

UC1
SA0000EQD0L
QY4U@
S IC A31 FJ8071504661121 QY4T Q0 1.2G S

ADL CPU QS

UC1
SA0000FE20L
Q0EZ@
S IC A31 FJ8071504827101 Q0EZ R0 1.2G S

UC1
SA0000FB71L
Q0EP@
S IC A31 FJ8071504826802 Q0EP R0 1.3G S

UC1
SA0000FE10L
Q0EQ@
S IC A31 FJ8071504826803 Q0EQ R0 1.3G S

UC1
SA0000FB51L
Q0E8@
S IC A31 FJ8071504826607 Q0E8 R0 1.7G S

UC1
SA0000FE00L
Q0EW@
S IC A31 FJ8071504827200 Q0EW R0 1.2G S

UC1
SA0000FE10L
Q0EX@
S IC A31 FJ8071504827201 Q0EX R0 1.2G S

UC1
SA0000FBR1L
Q0EV@
S IC A31 FJ8071504827100 Q0EV R0 1.2G S

UC1
SA0000FE30L
Q0EY@
S IC A31 FJ8071504827300 Q0EY R0 1.1G S

ADL CPU MP R3

UC1
SA0000FBR3L
I31215@
S IC FJ8071504827100 SRLFT R0 1.2G A31 !

UC1
SA0000FB73L
I51235@
S IC FJ8071504826802 SRLFQ R0 1.3G A31 !

UC1
SA0000FB53L
I71255@
S IC FJ8071504826607 SRLFP R0 1.7G A31 !

UC1
SA0000FE02L
P8505@
S IC FJ8071504827200 SRLFV R0 1.2G A31 !

UC1
SA0000FE32L
C7305@
S IC FJ8071504827300 SRLFX R0 1.1G A31 !

@ : Un-pop Component
UMA@ : not Support external Graphic card
N3@/V3@ : Inspiron/Vostro
MSFT@/NMSFT@ : MSFT SKU / Normal SKU
G3@ : Support G3 sharing SPI topology
CNV@ : Support CNVi function
S5LID@/LID@ : Support S5 LID power up Function/Normal LID close
ES_I3@/ES_I5A@/ES_I5B@/QS_I7@ : TGL-U QS Sample
STG@ : C10_gate control VCCSTG
I2CTCH@/USBTCH@ : Touch Screen support I2C signal / USB signal
BASE@/PREM@ : Pentium,Celeron/i3,i5,i7
I2CPAD@/PS2PAD@ : EC use I2C touch PAD signal(or PS2)
JP@/JUMP@/PJP@ : JUMP
100@/1000@ : 10/100 LAN / Giga-LAN
PRO@/ICPRO@ : only LCDVDD protection/Hinge up protection Support
EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
CMC@ : XDP Component
CONN@ : Connector Component
KBBL@ : KB Backlight
TPM@/NTPM@ : HW TPM/SW TPM
750_CTPM@ : 750 and china TPM
CTPM@/ST_CTPM@ : China TPM/ST China TPM
FFS@ : Free Fall Sensor
TYPEC@/NTYPEC@ : Support TypeC/non-TypeC
TYPEC@EMI@/TYPEC@ESD@ : EMI, ESD ,TypeC Component
LBIST@/LBIST@RF@ : LBIST for LCD monitor
TP@/CMC@TP@ : Test Point/XDP Test Point
DISPCB@/UMAPCB@ : PCB MB

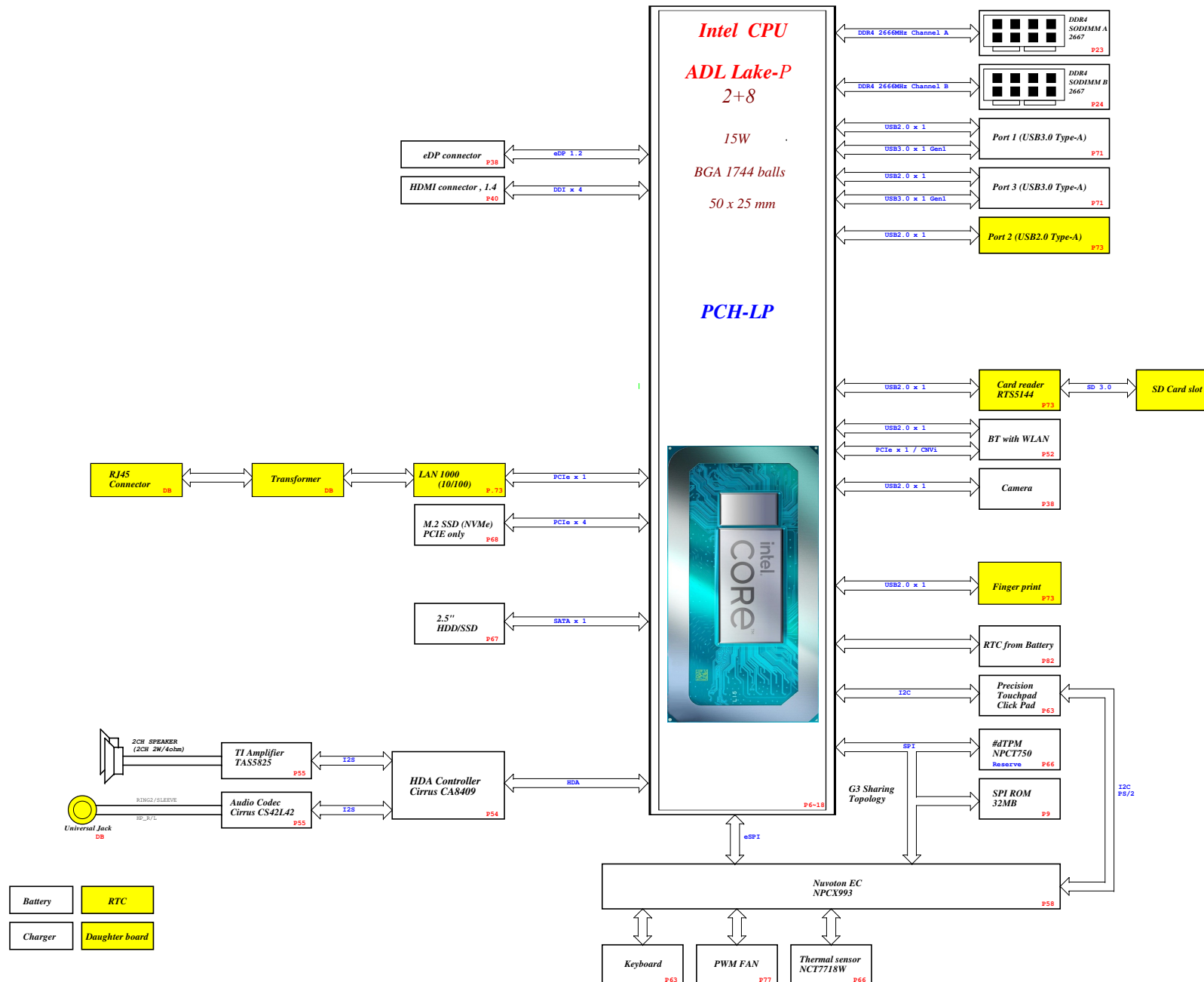
Layout Dell logo



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Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title	Cover Page	
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					LA-L946P	1.0
				Date:	Friday, April 08, 2022	Sheet 1 of 121

Block Diagram



Signal State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	---	---	---	---	---	---	---

USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 Port2
3	USB2.0 port3, IO/B
4	NC
5	Finger printer
6	CCD
7	Card reader , IO/B
8	NC
9	NC
10	BT

Bullseye TGL			
NBDR	SKU	Model-ID (RE4 PD-100K)	Board-ID (RE2 PD-100K)
	UMA	RE3 PU-10K	RE1 PU-10K -EVT RE1 PU-17.8K -DVT1 RE1 PU-27.0K -Reserve RE1 PU-37.4K -DVT2 RE1 PU-49.9K -Reserve
	DSC - N175-G3	RE3 PU-17.8K	RE1 PU-64.9K Pilot RE1 PU-82.5K -Reserve

Power Plane	Description	S0	S3	S4/S5	G3
+19V_ADPIN	Adapter power supply	N/A	N/A	N/A	N/A
+17.4V_BATT+H	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for System	N/A	N/A	N/A	N/A
+RTC_SOC	RTC power	ON	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	OFF
+3VALW_DS	System +3V always on power rail	ON	ON	ON	OFF
+3VALW	System +3V always on power rail	ON	ON	ON	OFF
+1.8V_PRIM	System +1.8V always on power rail	ON	ON	ON	OFF
+1.0V_PRIM	System +1.0V always on power rail	ON	ON	ON	OFF
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	ON	ON	OFF
+VCCST	+1.05 VCCST power rail	ON	ON	ON	OFF
+VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF	OFF
VCCPLL	+1.05 VCCPLL power rail	ON	ON	ON	OFF
+VCC_IN	Core voltage for CPU	ON	OFF	OFF	OFF
+3VLP	+139VB to +3VLP power rail for suspend power	ON	ON	ON	OFF
+3VALW_DS	+139VB to DSW power rail for suspend power	ON	ON	ON	OFF
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	ON	OFF
+5VS	System +5VS power rail	ON	ON	OFF	OFF
+3VS	System +3VS power rail	ON	ON	OFF	OFF
+1.35V_MEM GFX	+1.35V power rail for GPU	ON	OFF	OFF	OFF
+3VG5	+3V power rail for GPU	ON	OFF	OFF	OFF
+1.8VG5	+1.8V power rail for GPU	ON	OFF	OFF	OFF
+0.95VSDGPU	+0.95V power rail for GPU	ON	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

寄件日期: 2019/6/6 (週四) 下午 09:41
收件者: Chio, David (TPE); Chen, Johnny (TPE); Hung, Henry (TPE); Chang, Jay Si; Liu, Joe (TPE); Lai, Carol (TPE); Kenny.Lu@del.com
副本: Chen, AlexCL (TPE); Chang, Garyl; Hsiao, Jimmy

Best Regards,
Eddie Wu +886-2-66221110

Rails	S/K Us	S0/ M0 ³	C10 ³	S0ix/ M-off ⁴	S3/M 3	S3/ M-off	S4 and S5/M 3	S4 and S5/M- off	Deep S4/S5	pseudoG3 ¹	True G3 ¹
VCCRTC	All	ON	ON	ON	ON	ON	ON	ON	ON	ON	No Power
VCCDSW_3P3	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power	No Power
VBATA (VDC)	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power	No Power
VCCPRIM_3P3	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power	No Power
VCCPRIM_1P8	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power	No Power
VCC_VNNEXT_1P05	P	ON	ON	ON	ON	ON	ON	ON	OFF	No Power	No Power
VCC_V1P05EXT_1P05	P	ON	ON	ON	ON	ON	ON	ON	OFF	No Power	No Power
V3.3M ⁵	All	ON	ON	OFF	ON ¹⁰	OFF	ON ¹⁰	OFF	OFF	No Power	No Power
V1.8M ⁵	All	ON	ON	OFF	ON ¹⁰	OFF	ON ¹⁰	OFF	OFF	No Power	No Power
VDD2	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power	No Power
VPP	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power	No Power
VCC1P05_PROC	All	ON	ON	ON	ON/O FF 12, 13	ON/O FF 12, 13	ON/O FF 12, 13	ON/O F 12, 13	OFF	No Power	No Power
VCCIN_AUX	All	ON	ON ¹⁴ / OFF2	ON ¹⁴ / OFF	ON ¹⁴ / OFF	ON ¹⁴ / OFF	ON ¹⁴ / OFF	ON ¹⁴ / OFF	OFF	No Power	No Power
VCC1P8_PROC	P	ON	ON ¹⁵ / OFF2	ON ¹⁵ / OFF2	ON ¹⁵ / OFF	ON ¹⁵ / 2/OFF F	ON ¹⁵ / OFF	ON ¹⁵ / OFF	OFF	No Power	No Power
VCC_MIP1LP19	P	ON	OFF ¹⁸	OFF ¹⁸	OFF	OFF	OFF	OFF	OFF	No Power	No Power

Rails	SK Us	S0/ M0 ³	C10 ²	S0ix/ M-off ⁴	S3/M 3	S3/ M-off	S3 and S5/M 3	S5/ M-off	Deep S4/S5	pseudoG3 ¹	True G3 ¹
VCCCORE	All	ON	OFF ¹⁷	OFF	OFF	OFF	OFF	OFF	OFF	No Power	No Power
VCCGT	All	ON	OFF ¹⁷	OFF	OFF	OFF	OFF	OFF	OFF	No Power	No Power

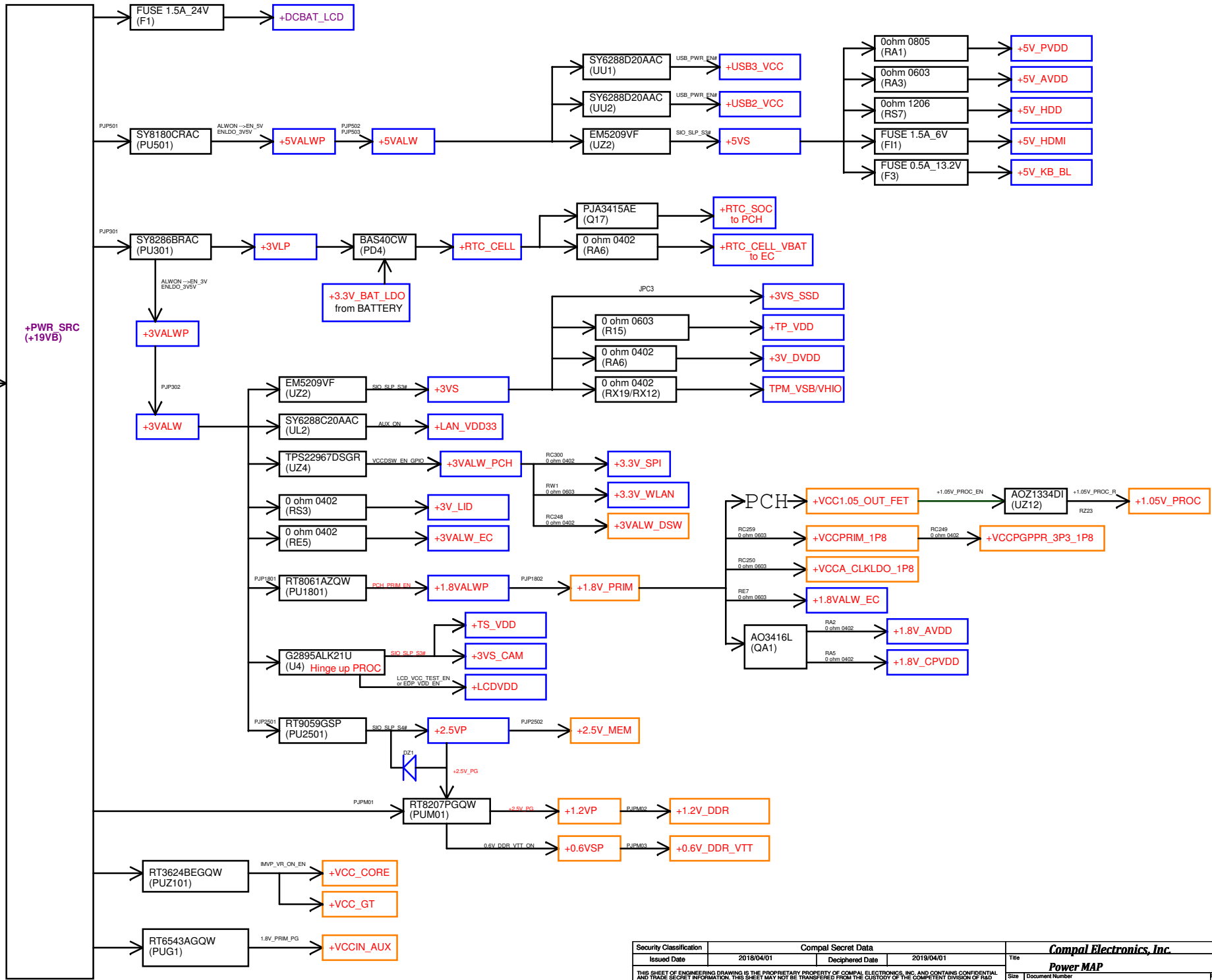
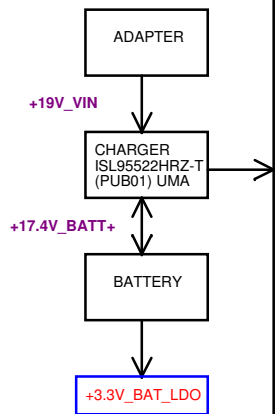
PCIe																					
Processor PCIe								PCH PCIe													
1	2	3	4	1	2	3	4	1	2	3	4	5	6	7	8	9	10	11	12		
PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe		
PCIe X4 Gen4				PCIe X4 Gen4				X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1	X1		
dGPU (GN18-S5) 1				M.2 SSD Gen4 1				M/B USB-A	M/B USB-A	M/B USB-A				M.2 SSD Gen3 2				LAN	WLAN	HDD	X1

Processor USB				USB 2.0										DDI	
1	2	3	4	1	2	3	4	5	6	7	8	9	10	1	2
TCP	TCP	TCP	TCP	USB2	USB2	USB2	USB2	USB2	USB2	USB2	USB2	USB2	USB2	DDI A	DDI B
TBT/USB4		TBT/USB4		USB2	USB2	USB2	USB2	USB2	USB2	USB2	USB2	USB2	USB2	eDP	eDP/HDMI
		Type-C DP	M/B USB-A	M/B USB-A	M/B USB-A IO/B	Type-C	Finger print	Camera	Card reader				BT	LCD	HDMI

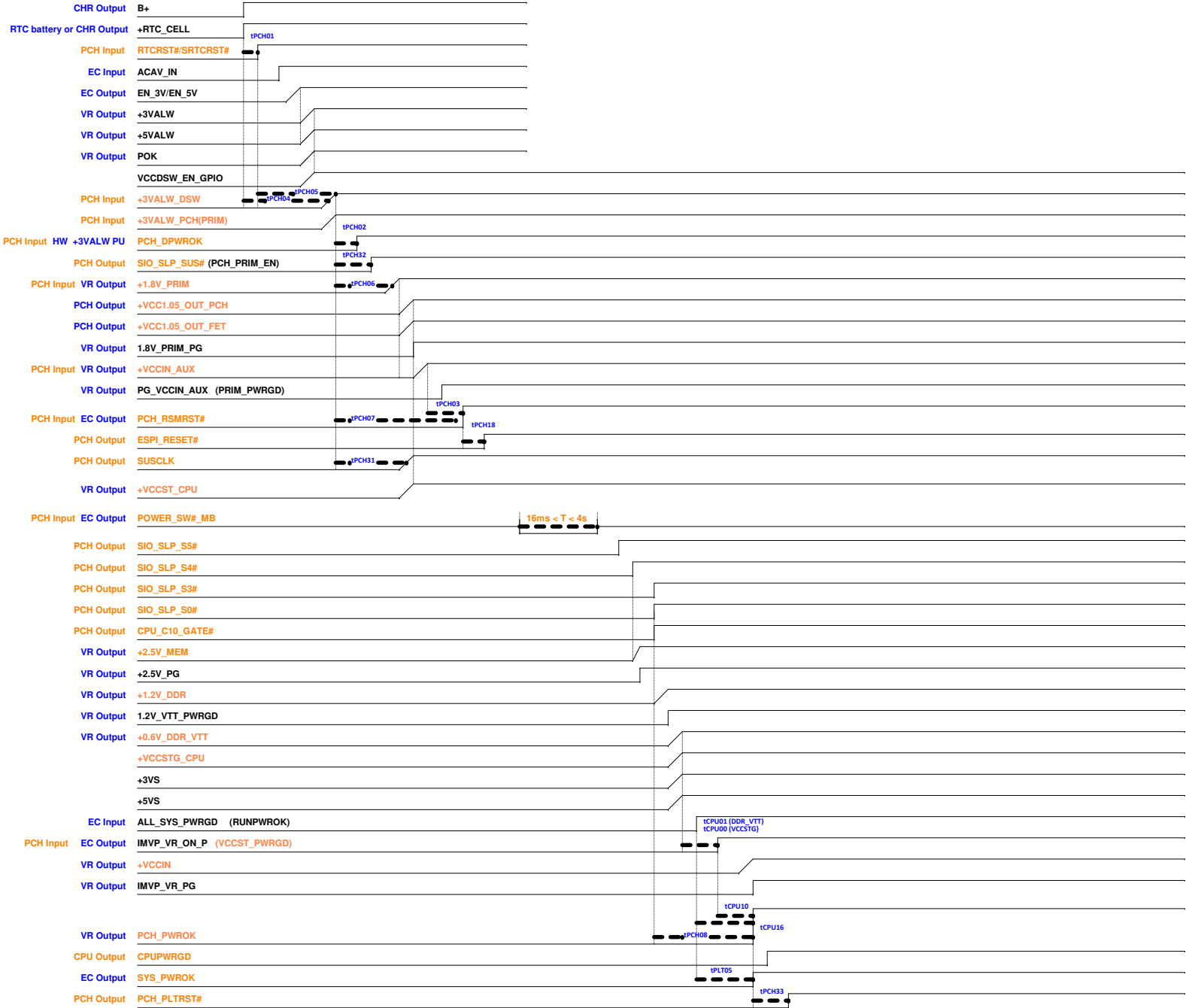
1. Only for UMA/DSC(8L)
2. Only for UMA(6L)

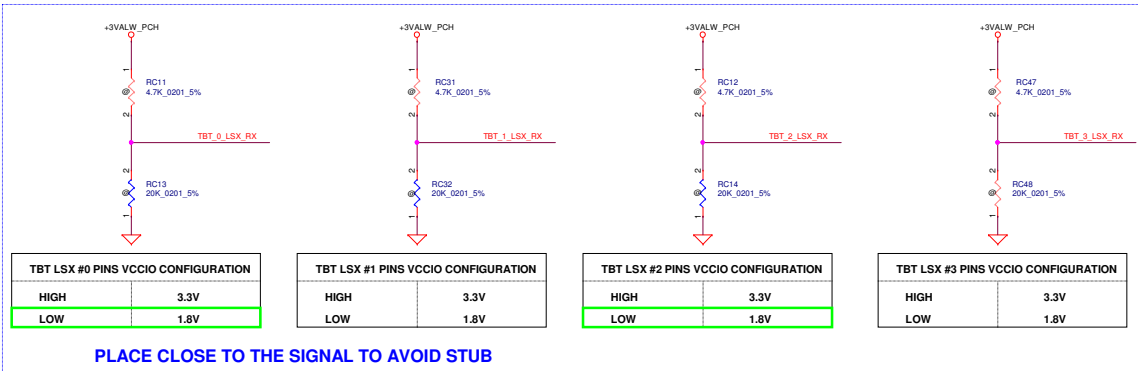
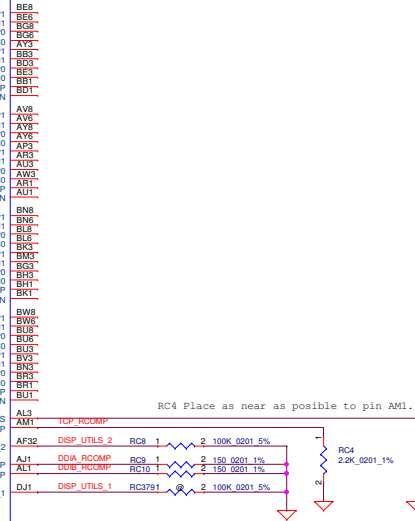
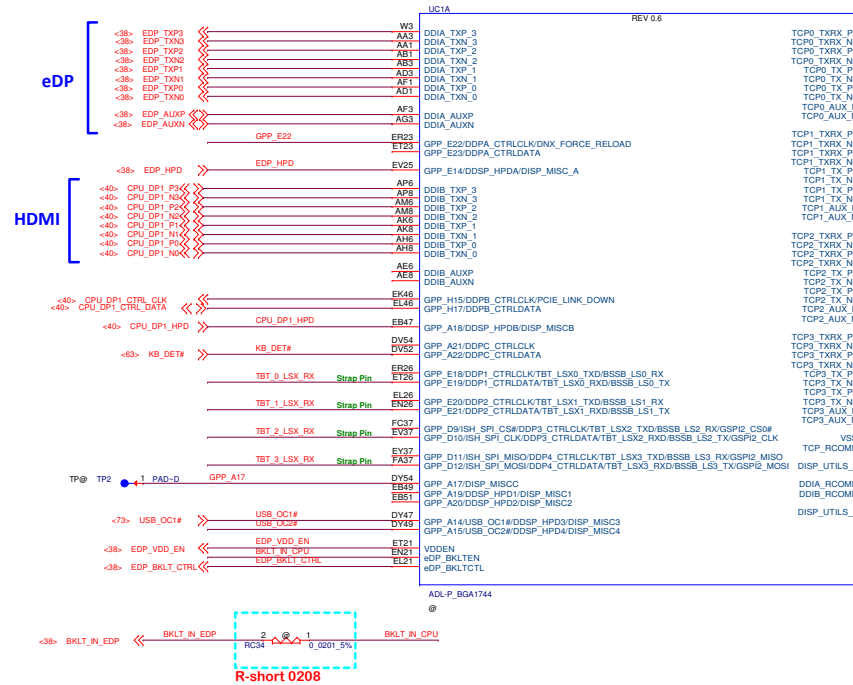
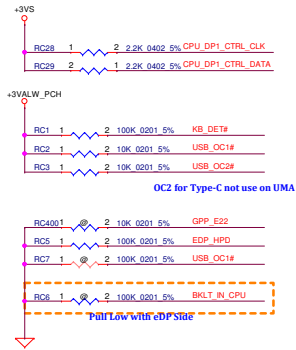
USB3.0	PCIE	SATA	DESTINATION
USB3.0-1	PCIE-1		USB3.0 (MB)(Type-A)
USB3.0-2	PCIE-2		USB3.0 (MB)(Type-A)
USB3.0-3	PCIE-3		NC
USB3.0-4	PCIE-4		NC
	PCIE-5		PCIE SSD
	PCIE-6		PCIE SSD
	PCIE-7		PCIE SSD
	PCIE-8		PCIE SSD
	PCIE-9		LOM
	PCIE-10		WLAN
	PCIE-11	SATA-0	SATA HDD
	PCIE-12		NC
	PCIE4 - 0		NC
	PCIE4 - 1		NC
	PCIE4 - 2		NC
	PCIE4 - 3		NC

Adapter/Battery/19V
CPU PWR
GPU PWR
Peripheral Device PWR



Power Up Sequence
G3 to S0



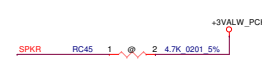


TOP SWAP OVERRIDE

GPP_B14 / SPKR (Internal 20 K Pull Down)

0 = Disable "Top Swap" mode. (Default)

1 = Enable "Top Swap" mode.

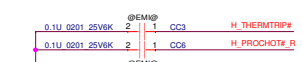
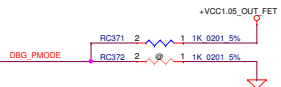


DFXTESTMODE(ITP_PMODE)

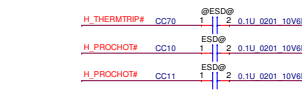
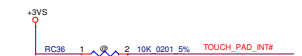
DBG_PMODE (Internal 20 K Pull UP)

0 = DFXTESTMODE ENABLED

1 = DFXTESTMODE DISABLED(DEFAULT)



EMI request, Place near CPU side.

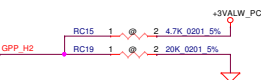


ESD Request: CC944 place near to RC37
CC945 place near to DC5
CC70 place near to M5

BOOT STRAP 3

GPP_H2 (Weak internal PD 20K)

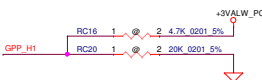
This is bit 3 of a total of 4-bit encoded pin straps for boot configuration.



BOOT STRAP 2

GPP_H1 (Weak internal PD 20K)

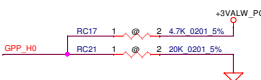
This is bit 2 of a total of 4-bit encoded pin straps for boot configuration.



BOOT STRAP 1

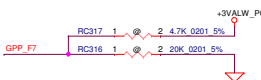
GPP_H0 (Weak internal PD 20K)

This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.



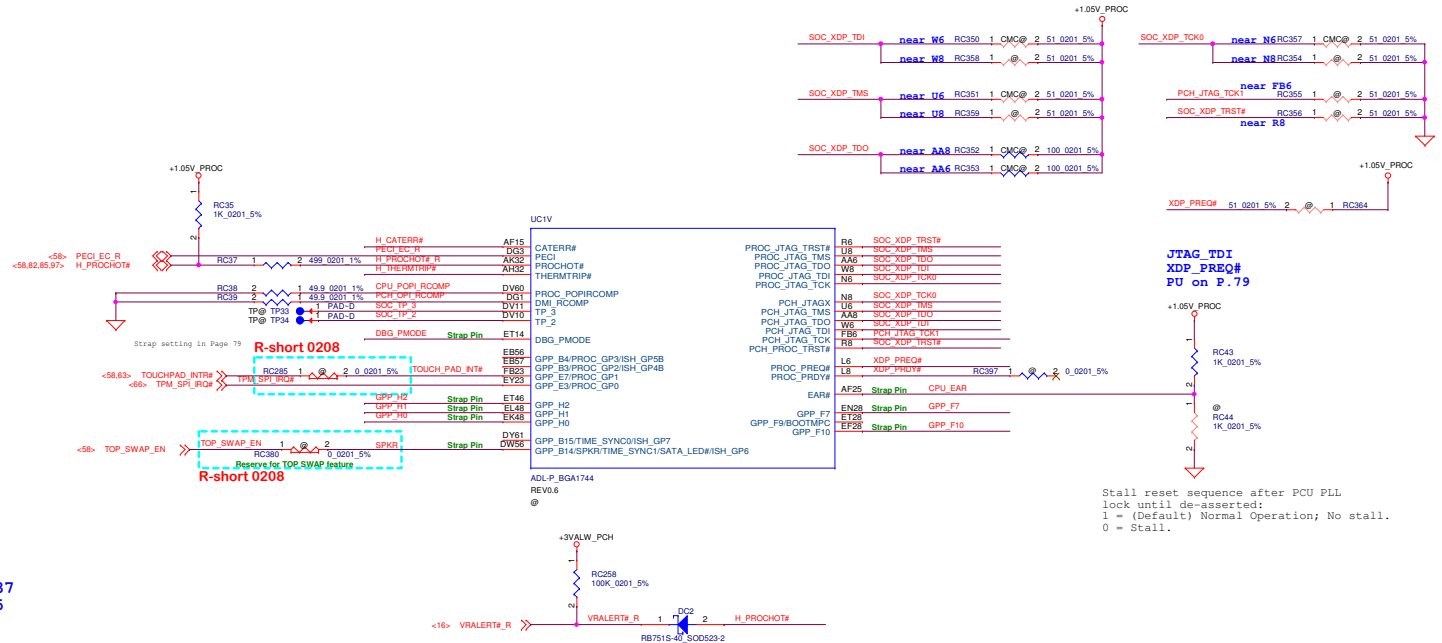
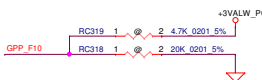
Reserved

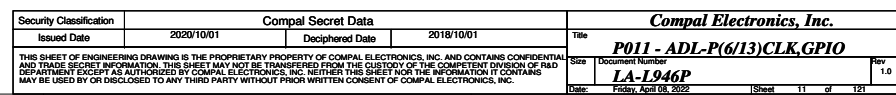
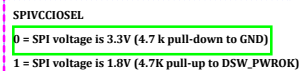
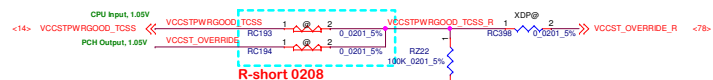
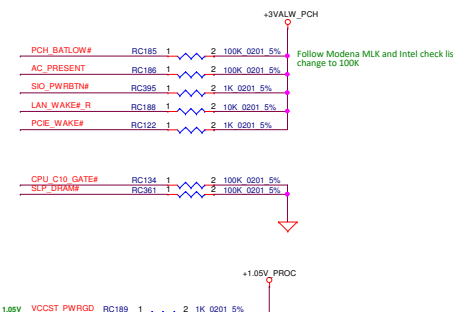
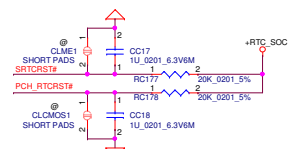
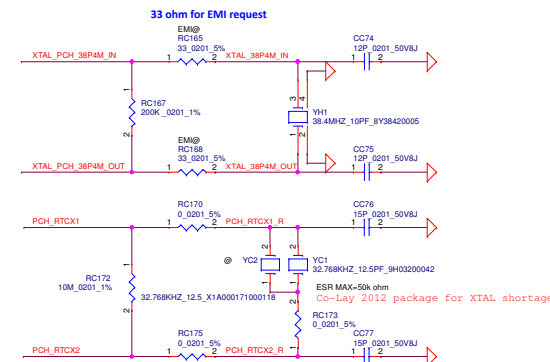
GPP_F7 (Weak internal PD 20K)



Reserved

GPP_F10 (Weak internal PD 20K)





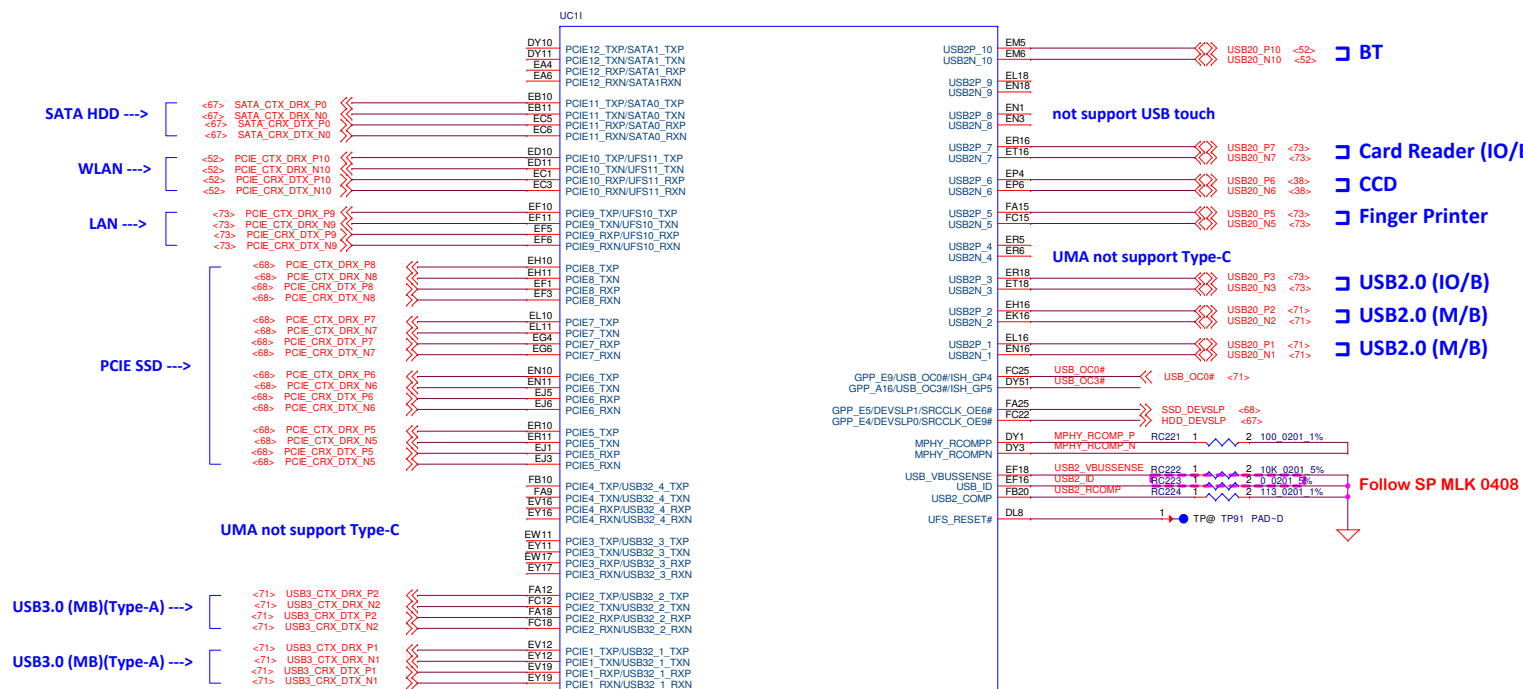
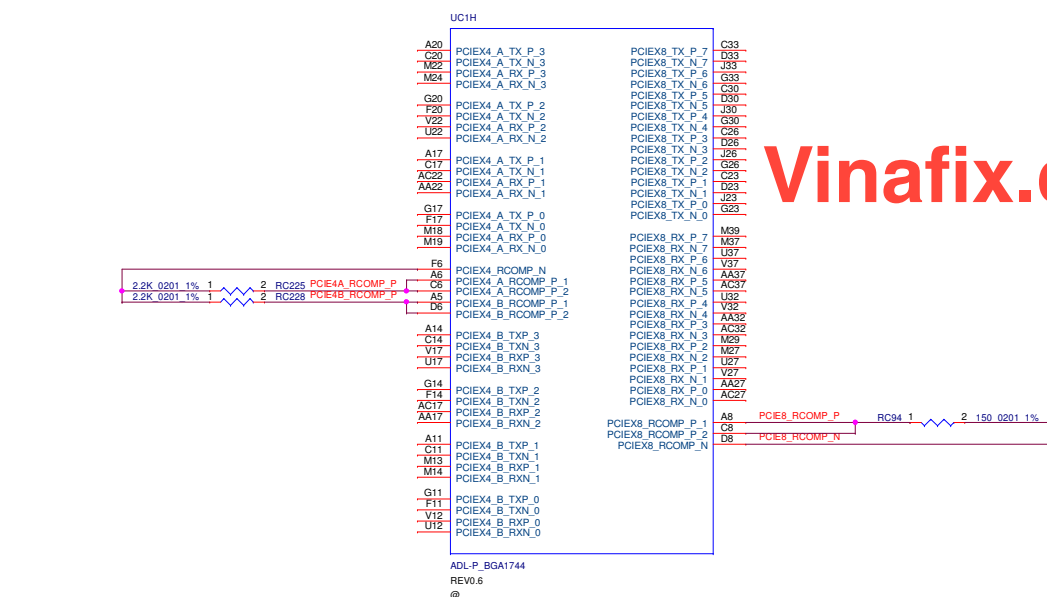
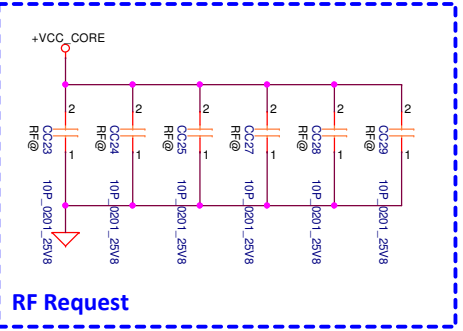
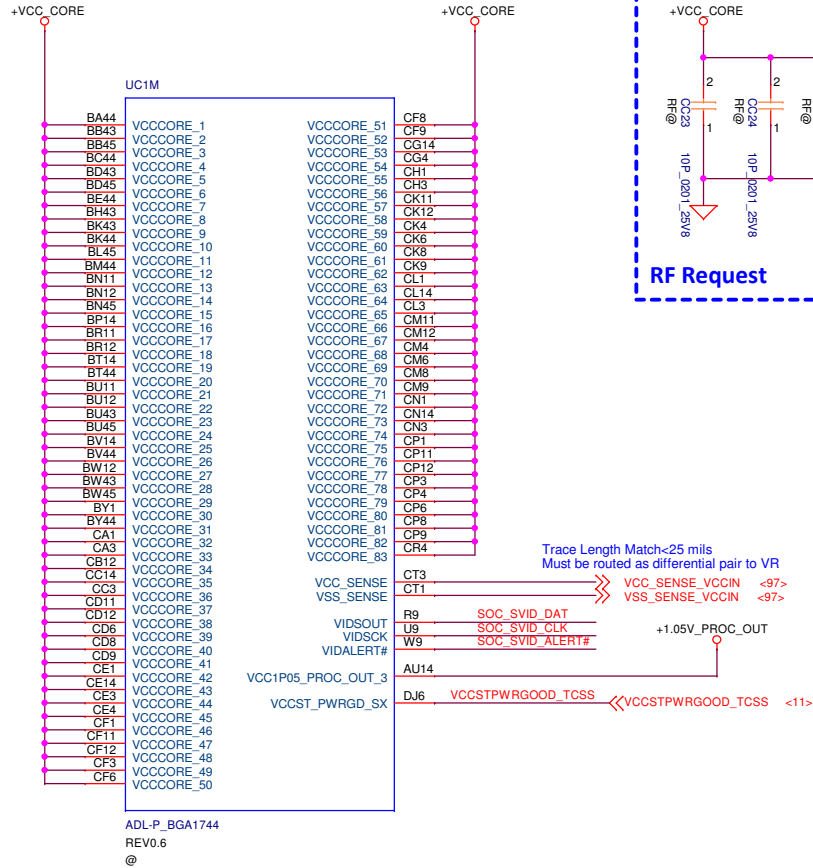


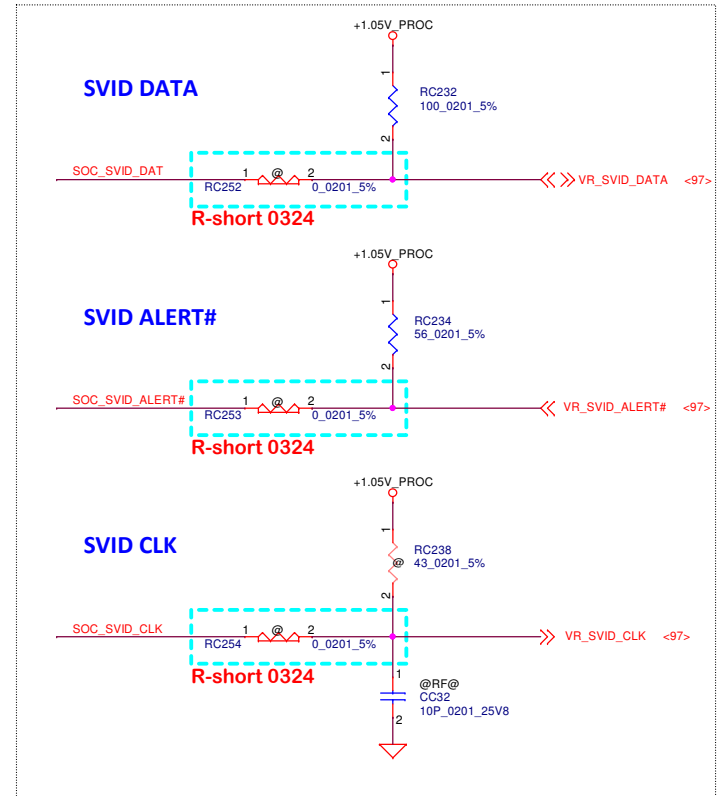
Figure 156. Supported PCH PCI Express* Link Configurations

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
Flex I/O Lanes		0	1	2	3	4	5	6	7	8	9	10	11
PCIe* Lanes		1	2	3	4	5	6	7	8	9	10	11	12
Link Lanes	1x4	0	1	2	3	0	1	2	3	0	1	2	3
	1x4 LR	3	2	1	0	3	2	1	0	3	2	1	0
	2x2	0	1	0	1	0	1	0	1	0	1	0	1
	1x2+2x1	0	1	0	0	0	1	0	0	0	1	0	0
	2x1+1x2	0	0	1	0	0	0	1	0	0	0	1	0
	4x1	0	0	0	0	0	0	0	0	0	0	0	0
Base-U	1x4					RP5				RP9			
	1x4 LR					RP5				RP9			
	2x2					RP5		RP7		RP9		RP11	
	1x2+2x1					RP5		RP7		RP9		RP11	
	2x1+1x2					RP8		RP7		RP5		RP9	
	4x1					RP5		RP6		RP7		RP8	
Premium-U	1x4	RP1				RP5				RP9			
	1x4 LR	RP1				RP5				RP9			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11	
	1x2+2x1	RP1		RP3		RP5		RP7		RP9		RP11	
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12
Premium-Y	1x4	RP1								RP9			
	1x4 LR	RP1								RP9			
	2x2	RP1		RP3				RP7		RP9		RP11	
	1x2+2x1	RP1		RP3				RP7		RP9		RP11	
	2x1+1x2	RP4	RP3	RP1						RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4			RP7		RP8	RP9	RP10	RP11

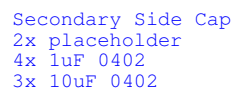




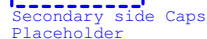
- 1.The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
 - 2.Route the Alert signal between the Clock and the Data signals.
- CAD Note: Place the PU resistors close to CPU



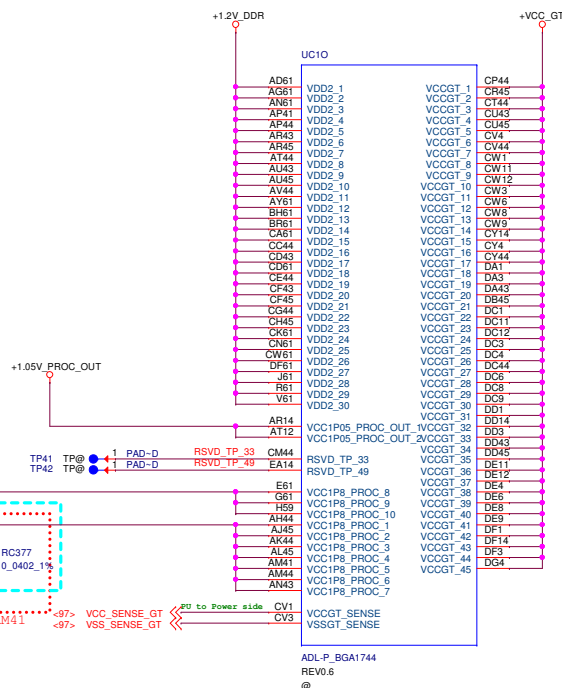
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						Size		Document Number		Rev	
						LA-L946P		1.0			
						Date:		Friday, April 08, 2022		Sheet 14 of 121	



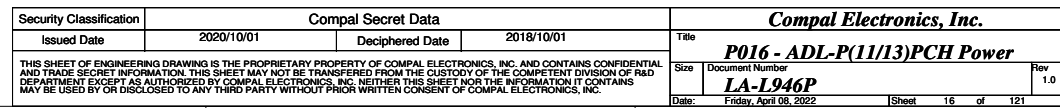
Primary side Caps



Follow Intel PDG and FAE reply
If not use PEG 010 port , VCC1P8 PROC can be connected to GND



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UC1R			
DC47	VSS_295	VSS_369	ED58
DC54	VSS_296	VSS_370	ED6
DC57	VSS_297	VSS_371	ED60
DC59	VSS_298	VSS_372	ED8
DE44	VSS_299	VSS_373	EE16
DE51	VSS_300	VSS_374	EE31
DE55	VSS_301	VSS_375	EE51
DF43	VSS_302	VSS_376	EF13
DF46	VSS_303	VSS_377	EF8
DF48	VSS_304	VSS_378	EH13
DF58	VSS_305	VSS_379	EH8
DG11	VSS_306	VSS_380	EK21
DG12	VSS_307	VSS_381	EK28
DG51	VSS_308	VSS_382	EK36
DG55	VSS_309	VSS_383	EK43
DG6	VSS_310	VSS_384	EK51
DG8	VSS_311	VSS_385	EK56
DG9	VSS_312	VSS_386	EK58
DH4	VSS_313	VSS_387	EL13
DH54	VSS_314	VSS_388	EL4
DJ47	VSS_315	VSS_389	EL8
DJ59	VSS_316	VSS_390	EN13
DK14	VSS_317	VSS_391	EN13
DK54	VSS_318	VSS_392	EN8
DL10	VSS_319	VSS_393	ER1
DL11	VSS_320	VSS_394	ER13
DL13	VSS_321	VSS_395	ER21
DM4	VSS_322	VSS_396	ER28
DM41	VSS_323	VSS_397	ER3
DM46	VSS_324	VSS_398	ER36
DM48	VSS_325	VSS_399	ER43
DM51	VSS_326	VSS_400	ER51
DM55	VSS_327	VSS_401	ER61
DM58	VSS_328	VSS_402	ER8
DM6	VSS_329	VSS_403	EU11
DM61	VSS_330	VSS_404	EU11
DN13	VSS_331	VSS_405	EUS8
DN40	VSS_332	VSS_406	EUS8
DN8	VSS_333	VSS_407	EV14
DP46	VSS_334	VSS_408	EV20
DP49	VSS_335	VSS_409	EV26
DT13	VSS_336	VSS_410	EV33
DT52	VSS_337	VSS_411	EV39
DT8	VSS_338	VSS_412	EV4
DV13	VSS_339	VSS_413	EV45
DV4	VSS_340	VSS_414	EV52
DV44	VSS_341	VSS_415	EV59
DV49	VSS_342	VSS_416	EW61
DV56	VSS_344	VSS_417	EY14
DV58	VSS_345	VSS_418	EY20
DV6	VSS_346	VSS_419	EY26
DV8	VSS_347	VSS_420	EY3
DW14	VSS_348	VSS_421	EY33
DW25	VSS_349	VSS_422	EY39
DW35	VSS_350	VSS_423	EY4
DY13	VSS_351	VSS_424	EY45
DY33	VSS_352	VSS_425	EY52
DY36	VSS_353	VSS_426	EY56
DY38	VSS_354	VSS_427	EY58
DY52	VSS_355	VSS_428	EY59
DY8	VSS_356	VSS_429	EY6
E43	VSS_357	VSS_430	EY9
E50	VSS_358	VSS_431	F21
EB13	VSS_359	VSS_432	F23
EB26	VSS_360	VSS_433	F26
EB31	VSS_361	VSS_434	F28
EB8	VSS_362	VSS_435	F30
EC21	VSS_363	VSS_436	F33
EC28	VSS_364	VSS_437	F34
ED13	VSS_365	VSS_438	F40
ED4	VSS_366	VSS_439	F46
ED56	VSS_367	VSS_440	F47
	VSS_368	VSS_441	F52
		VSS_442	

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UC1S			
F56	VSS_443	VSS_517	M36
F59	VSS_444	VSS_518	M47
F9	VSS_445	VSS_519	M57
FA40	VSS_446	VSS_520	M59
FA7	VSS_447	VSS_521	N1
FB1	VSS_448	VSS_522	N4
FB14	VSS_449	VSS_523	N41
FB26	VSS_450	VSS_524	N48
FB42	VSS_451	VSS_525	N54
FB48	VSS_452	VSS_526	N9
FB59	VSS_453	VSS_527	P11
FB61	VSS_454	VSS_528	P16
FC2	VSS_455	VSS_529	P21
FC55	VSS_456	VSS_530	P26
FC56	VSS_457	VSS_531	P3
FC58	VSS_458	VSS_532	P31
FC60	VSS_459	VSS_533	P35
G21	VSS_460	VSS_534	P47
G25	VSS_461	VSS_535	P51
G28	VSS_462	VSS_536	P55
G31	VSS_463	VSS_537	R12
G34	VSS_464	VSS_538	R17
G42	VSS_465	VSS_539	R22
G43	VSS_466	VSS_540	R27
G50	VSS_467	VSS_541	R32
H1	VSS_468	VSS_542	R37
H13	VSS_469	VSS_543	R44
H16	VSS_470	VSS_544	R48
H18	VSS_471	VSS_545	R58
H34	VSS_472	VSS_546	T1
H37	VSS_473	VSS_547	T11
H62	VSS_474	VSS_548	T16
H58	VSS_475	VSS_549	T21
H6	VSS_476	VSS_550	T26
H8	VSS_477	VSS_551	T3
H9	VSS_478	VSS_552	T35
J11	VSS_479	VSS_553	T36
J14	VSS_480	VSS_554	T40
J17	VSS_481	VSS_555	T52
J20	VSS_482	VSS_556	U16
J21	VSS_483	VSS_557	U21
J25	VSS_484	VSS_558	U26
J28	VSS_485	VSS_559	U32
J31	VSS_486	VSS_560	U35
J36	VSS_487	VSS_561	U44
J39	VSS_488	VSS_562	U46
J47	VSS_489	VSS_563	V3
J48	VSS_490	VSS_564	V40
J51	VSS_491	VSS_565	V41
J55	VSS_492	VSS_566	V51
K4	VSS_493	VSS_567	V55
L12	VSS_494	VSS_568	V58
L13	VSS_495	VSS_569	W1
L15	VSS_496	VSS_570	W11
L17	VSS_497	VSS_571	W16
L18	VSS_498	VSS_572	W21
L20	VSS_499	VSS_573	W26
L22	VSS_500	VSS_574	W31
L23	VSS_501	VSS_575	W35
L27	VSS_502	VSS_576	W44
L30	VSS_503	VSS_577	Y4
L33	VSS_504	VSS_578	Y17
L35	VSS_505	VSS_579	Y22
L36	VSS_506	VSS_580	Y27
L38	VSS_507	VSS_581	Y32
L40	VSS_508	VSS_582	Y37
L54	VSS_509	VSS_583	Y43
L9	VSS_510	VSS_584	Y45
M16	VSS_511	VSS_585	Y47
M21	VSS_512	VSS_586	Y49
M26	VSS_513	VSS_587	Y54
M31	VSS_514	VSS_588	
M32	VSS_515		
M34	VSS_516		

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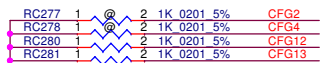
UC1P			
A3	VSS_7	VSS_74	AL15
A10	VSS_1	VSS_75	AL17
A21	VSS_2	VSS_76	AL22
A23	VSS_3	VSS_77	AL4
A25	VSS_4	VSS_78	AL41
A26	VSS_5	VSS_79	AN17
A28	VSS_6	VSS_80	AN40
A30	VSS_8	VSS_81	AN46
A31	VSS_9	VSS_82	AN48
A33	VSS_10	VSS_83	AN58
A40	VSS_11	VSS_84	AP1
A47	VSS_12	VSS_85	AP15
A53	VSS_13	VSS_86	AP20
A60	VSS_14	VSS_87	AP22
AA11	VSS_15	VSS_88	AP25
AA21	VSS_16	VSS_89	AP35
AA26	VSS_17	VSS_90	AP51
AA31	VSS_18	VSS_91	AT6
AA35	VSS_19	VSS_92	AT7
AA40	VSS_20	VSS_93	AT8
AA44	VSS_21	VSS_94	AT9
AA57	VSS_22	VSS_95	AT16
AA59	VSS_23	VSS_96	AT17
AB16	VSS_24	VSS_97	AT19
AB21	VSS_25	VSS_98	AT25
AB31	VSS_26	VSS_99	AT26
AB35	VSS_27	VSS_100	AT27
AB54	VSS_28	VSS_101	AT28
AC4	VSS_29	VSS_102	AT29
AC40	VSS_30	VSS_103	AT35
AC44	VSS_31	VSS_104	AT36
AC51	VSS_32	VSS_105	AT37
AC55	VSS_33	VSS_106	AT38
AC6	VSS_34	VSS_107	AT39
AC8	VSS_35	VSS_108	AT40
AD21	VSS_36	VSS_109	AT41
AD26	VSS_37	VSS_110	AT42
AD31	VSS_38	VSS_111	AT43
AD35	VSS_39	VSS_112	AT44
AD46	VSS_40	VSS_113	AT45
AD48	VSS_41	VSS_114	AT46
AD58	VSS_42	VSS_115	AT47
AE12	VSS_43	VSS_116	AT48
AE17	VSS_44	VSS_117	AT49
AE22	VSS_45	VSS_118	AT50
AE27	VSS_46	VSS_119	AT51
AE32	VSS_47	VSS_120	AT52
AE37	VSS_48	VSS_121	AT53
AE40	VSS_49	VSS_122	AT54
AE44	VSS_50	VSS_123	AT55
AE52	VSS_51	VSS_124	AT56
AE9	VSS_52	VSS_125	AT57
AF4	VSS_53	VSS_126	AT58
AF46	VSS_54	VSS_127	AT59
AG1	VSS_55	VSS_128	AT60
AG51	VSS_56	VSS_130	AT61
AG55	VSS_57	VSS_131	AT62
AG58	VSS_58	VSS_132	AT63
AG59	VSS_59	VSS_133	AT64
AH9	VSS_60	VSS_134	AT65
AJ3	VSS_61	VSS_135	AT66
AJ41	VSS_62	VSS_136	AT67
AJ47	VSS_63	VSS_137	AT68
AJ54	VSS_64	VSS_138	AT69
AK20	VSS_65	VSS_139	AT70
AK25	VSS_66	VSS_140	AT71
AK30	VSS_67	VSS_141	AT72
AK36	VSS_68	VSS_142	AT73
AK4	VSS_69	VSS_143	AT74
AK57	VSS_70	VSS_144	AT75
AK59	VSS_71	VSS_145	AT76
AK9	VSS_72	VSS_147	AT77
	VSS_73	VSS_148	AT78

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UC1Q			
BF58	VSS_149	VSS_222	CD58
BG1	VSS_150	VSS_223	CE51
BG12	VSS_151	VSS_224	CE55
BG44	VSS_152	VSS_225	CF47
BG52	VSS_153	VSS_226	CF49
BG9	VSS_154	VSS_227	CF54
BH4	VSS_155	VSS_228	CG57
BH46	VSS_156	VSS_229	CG59
BH48	VSS_157	VSS_230	CH11
BH58	VSS_158	VSS_231	CH12
BJ51	VSS_159	VSS_232	CH54
BJ55	VSS_160	VSS_233	CH6
BJ6	VSS_161	VSS_234	CH8
BL9	VSS_162	VSS_235	CH9
BL11	VSS_163	VSS_236	CJ14
BL4	VSS_164	VSS_237	CJ4
BL54	VSS_165	VSS_238	CJ44
BL9	VSS_166	VSS_239	CK1
BM1	VSS_167	VSS_240	CK3
BM14	VSS_168	VSS_241	CK43
BM47	VSS_169	VSS_242	CK46
BM57	VSS_170	VSS_243	CK48
BM59	VSS_171	VSS_244	CK51
BN54	VSS_172	VSS_245	CK55
BN54	VSS_173	VSS_246	CK59
BN9	VSS_174	VSS_247	CM52
BP4	VSS_175	VSS_248	CM58
BP51	VSS_176	VSS_249	CP51
BP55	VSS_177	VSS_250	CP55
BR43	VSS_178	VSS_251	CR43
BR46	VSS_179	VSS_252	CR47
BR48	VSS_180	VSS_253	CR49
BR58	VSS_181	VSS_254	CR54
BR6	VSS_182	VSS_255	CT11
BR8	VSS_183	VSS_256	CT16
BR9	VSS_184	VSS_257	CT57
BT14	VSS_185	VSS_258	CT59
BT51	VSS_186	VSS_259	CT6
BT55	VSS_187	VSS_260	CT8
BU54	VSS_188	VSS_261	CT9
BU9	VSS_189	VSS_262	CU4
BV1	VSS_190	VSS_263	CU54
BV47	VSS_191	VSS_264	CV14
BV57	VSS_192	VSS_265	CW43
BV59	VSS_193	VSS_266	CW46
BW4	VSS_194	VSS_267	CW48
BW54	VSS_195	VSS_268	CW51
BW9	VSS_196	VSS_269	CW55
BY3	VSS_197	VSS_270	CW58
C1	VSS_198	VSS_271	CY51
C21	VSS_199	VSS_272	D11
C25	VSS_200	VSS_273	D14
C28	VSS_201	VSS_274	D17
C31	VSS_202	VSS_275	D20
C34	VSS_203	VSS_276	D21
C40	VSS_204	VSS_277	D25
C47	VSS_205	VSS_278	D28
C9	VSS_206	VSS_279	D31
CA14	VSS_207	VSS_280	D4
CA43	VSS_208	VSS_281	D53
CA46	VSS_209	VSS_282	D56
CA48	VSS_210	VSS_283	D58
CA51	VSS_211	VSS_284	D59
CA55	VSS_212	VSS_285	D9
CA58	VSS_213	VSS_286	DA11
CB4	VSS_214	VSS_287	DA12
CB6	VSS_215	VSS_288	DA6
CB8	VSS_216	VSS_289	DA8
CB9	VSS_217	VSS_290	DA9
CC1	VSS_218	VSS_291	DB14
CC52	VSS_219	VSS_292	DB4
CC56	VSS_220	VSS_293	DB54
CD46	VSS_221	VSS_294	

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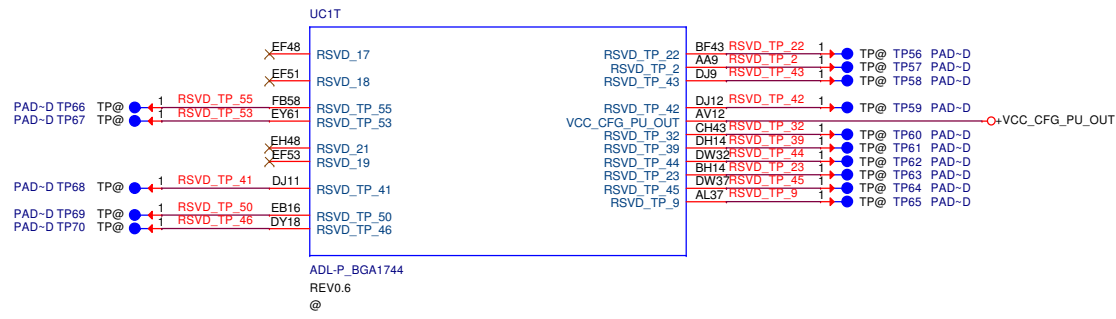
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CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull-Up to VCCIP05_PROG	1K ohm
CFG[0]	RSVD	None	
CFG[1]	RSVD	None	

[illegible]

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Notice:ADL-P RVP 1.8VS

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				Document Number	Rev
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				Date:	Friday, April 08, 2022	Sheet 20 of 121

Reserve

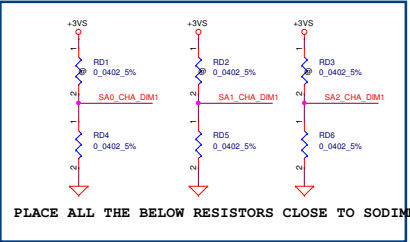
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Issued Date	2014/09/08	Deciphered Date	2013/10/28	Title	(RSVD)	
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CHANNEL-M0

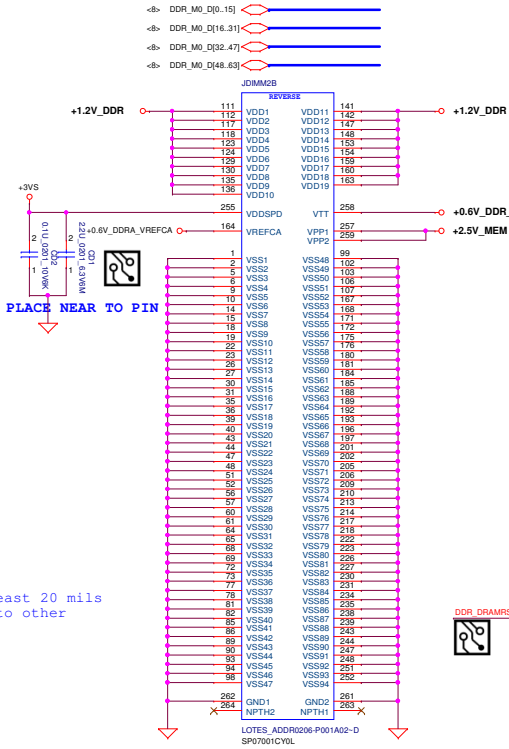
BOT: DIMM1(JDIMM2 CONN) Non-ECC DIMM



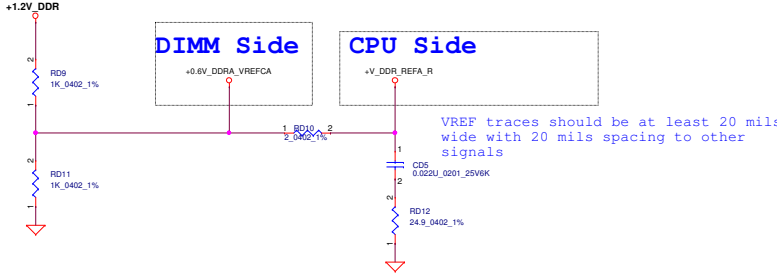
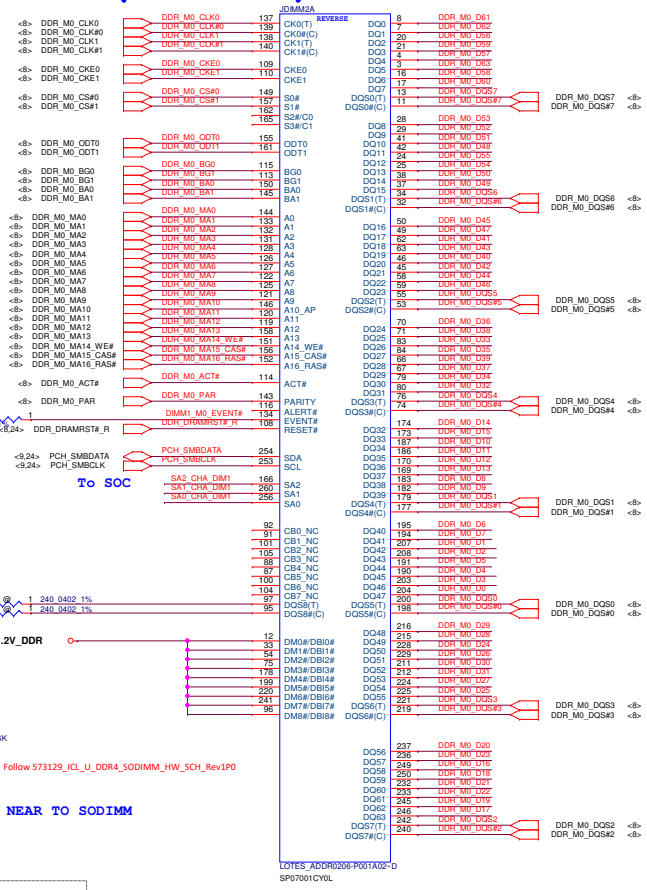
SPD ADDRESS FOR CHANNEL A :

SA0 = 0; SA1 = 0; SA2 = 0.

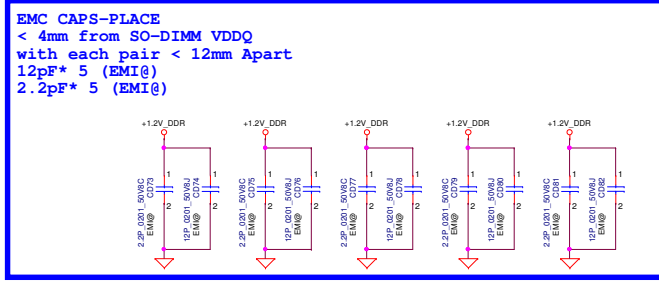
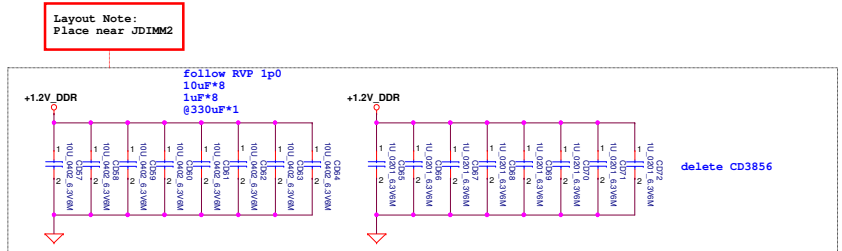
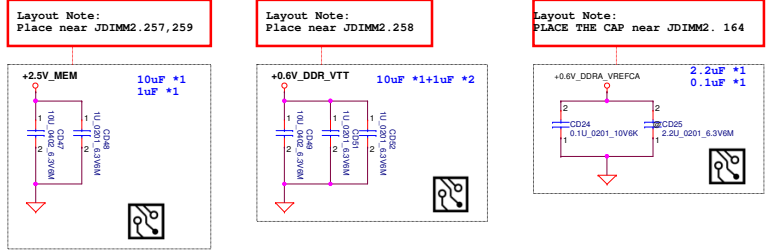
Non-Interleaved Memory



REVERSE TYPE (5.2 mm)

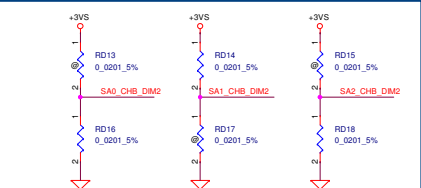


Decoupling Cap_Channel A



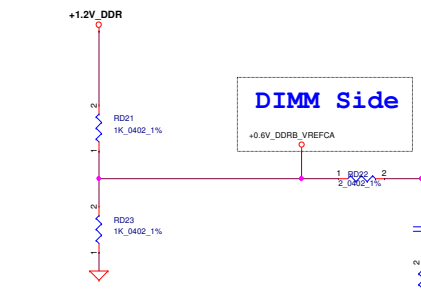
CHANNEL-M1

BOT: DIMM2 (JDIMM1 CONN) Non-ECC DIMM



PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
SA0 = 0; SA1 = 1; SA2 = 0.



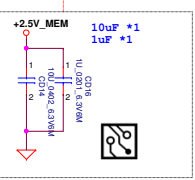
DIMM Side

CPU Side

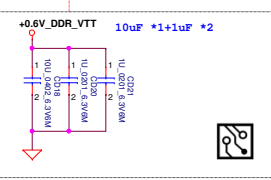
VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

Decoupling Cap_Channel B

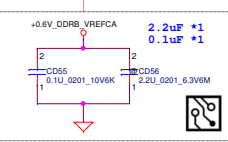
Layout Note:
Place near JDIMM1.257,259



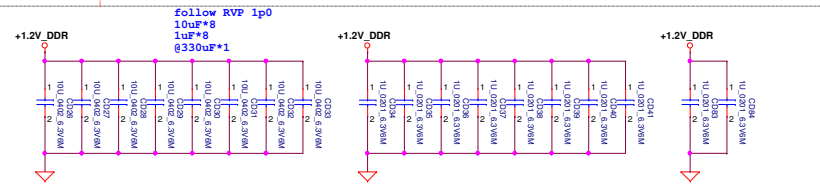
Layout Note:
Place near JDIMM1.258



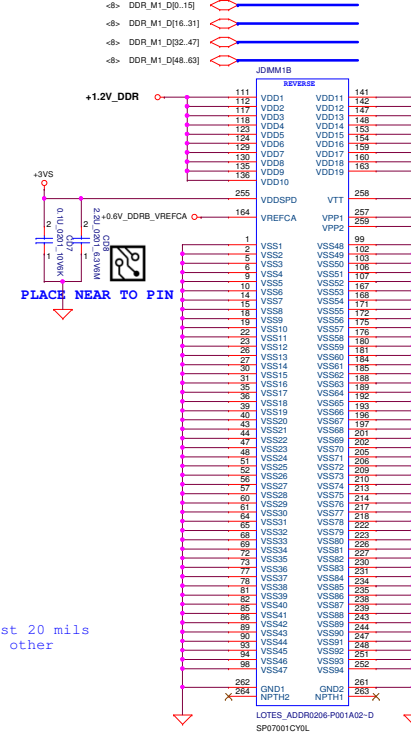
Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM1



Layout Note:
Place near JDIMM1

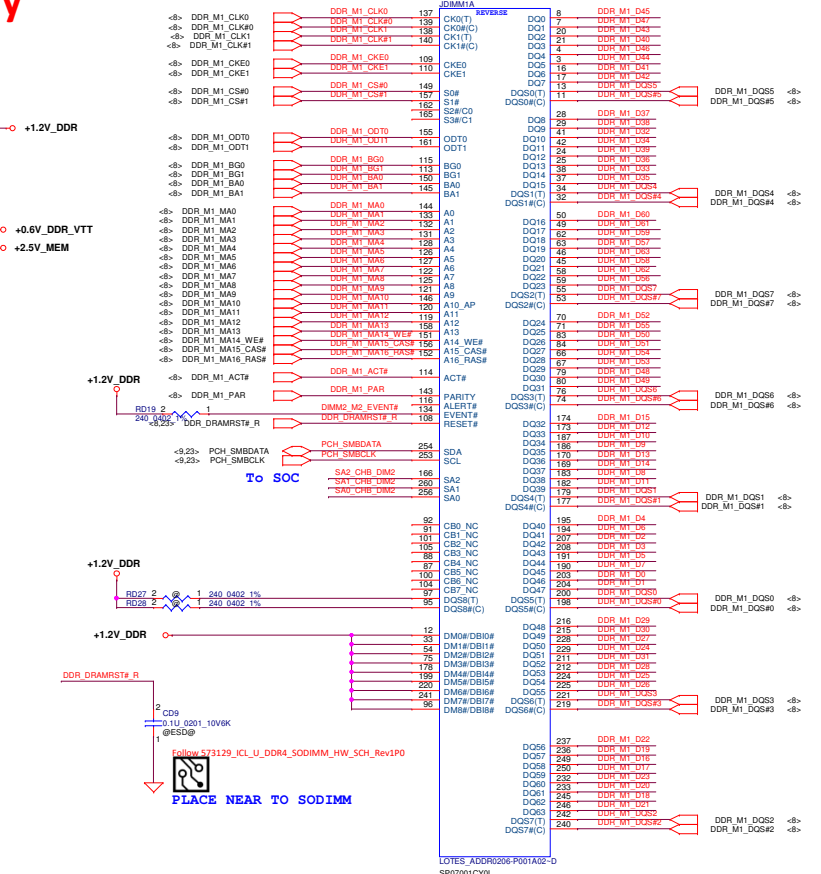


Non-Interleaved Memory



PLACE NEAR TO PIN

STD (5.2 mm)



To SOC

PLACE NEAR TO SODIMM

Part Number:SP07001HY00
Part Value:S SOCKET LOTES ADDR0207-P001A 260P DDR4

08/30
Update Table 4-26 for DDR4 SO-DIMM Decoupling Caps
572907_ICL_U4_PDG_Rev07 Page. 99

Table 4-26. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
DDR4 SODIMM 1DPC	VDDQ/VDD	4 near each side of the DIMM connector close to VDD pins	16x 10 μ F (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1 μ F (0402)
	VTT	Place on VTT plane close to DIMM	1x 330 μ F (7343)
		1 cap stuffed, 1 placeholder	2x 10 μ F (0603)
	VPP	Place on VTT plane close to DIMM	4x 1 μ F (0402)
		DIMM pin side, 1 per DIMM	2x 10 μ F (0603)
	VDDSPD	DIMM pin side, 1 per DIMM	2x 1 μ F (0402)
		Place close to DIMM	2x 0.1 μ F (0402)
		Place close to DIMM	2x 2.2 μ F (0402)

Note:
1. Total quantity is referring to 2 channels.

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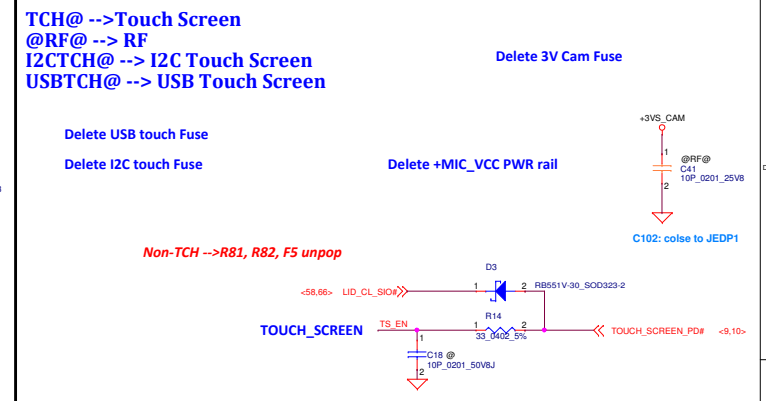
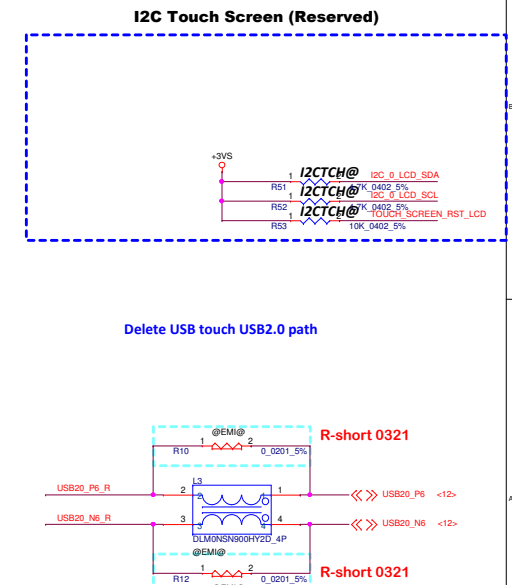
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2
Main Func = CAM&MIC, TS

[illegible]

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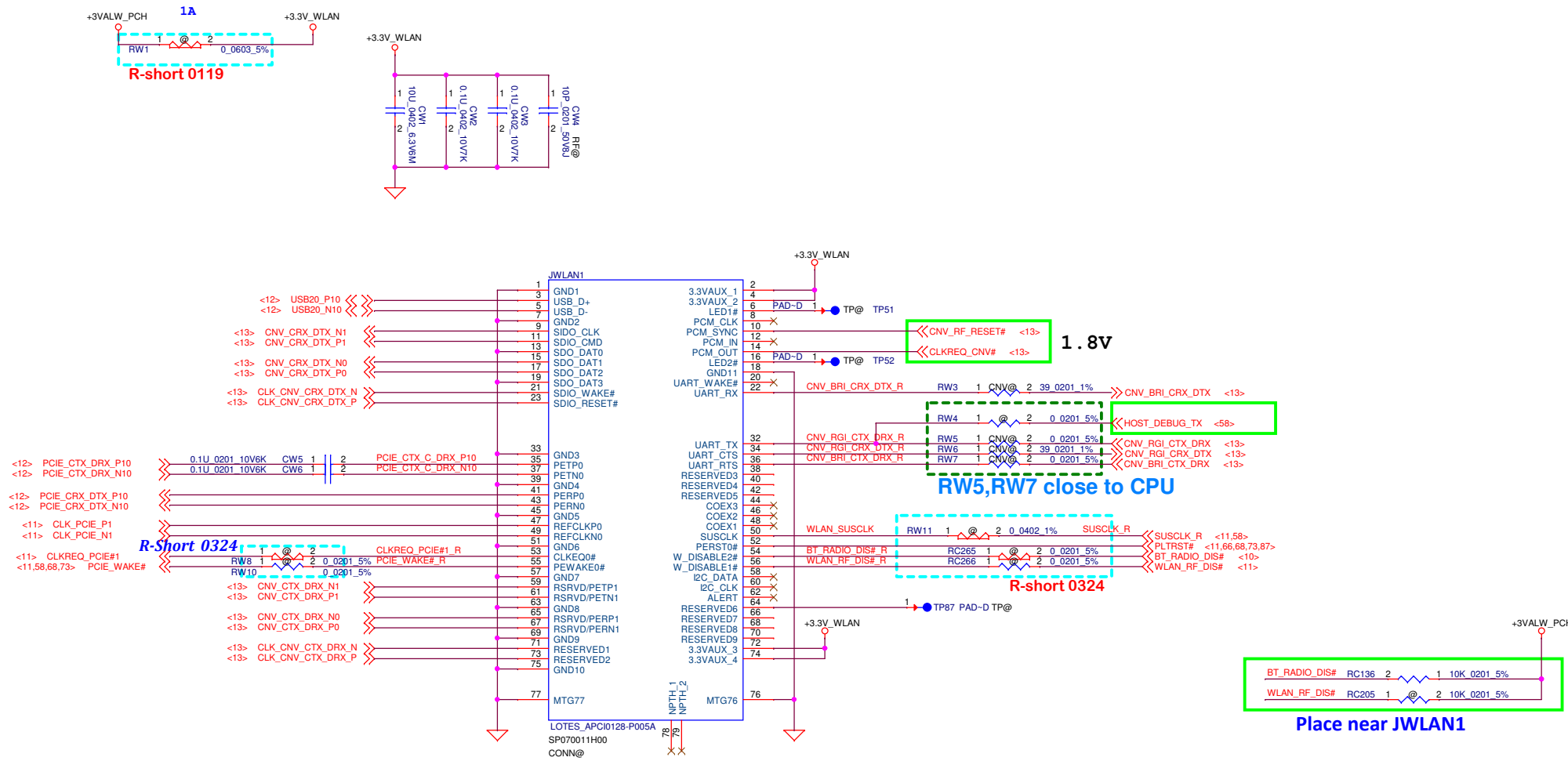
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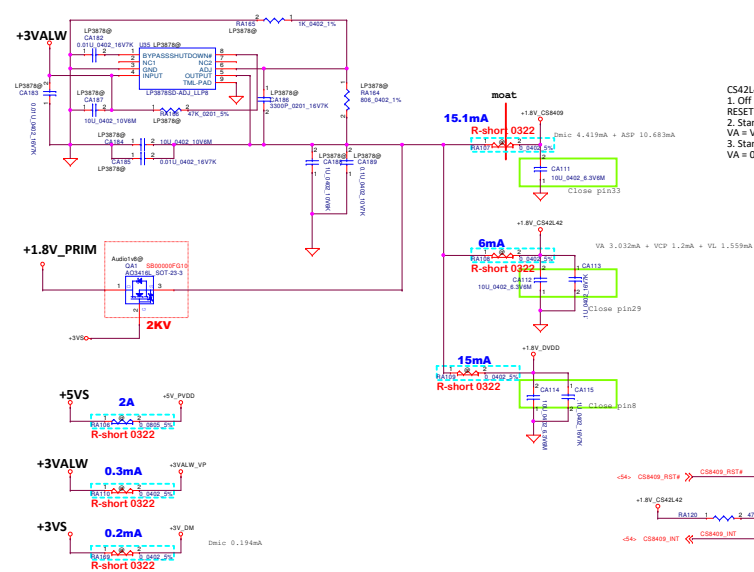
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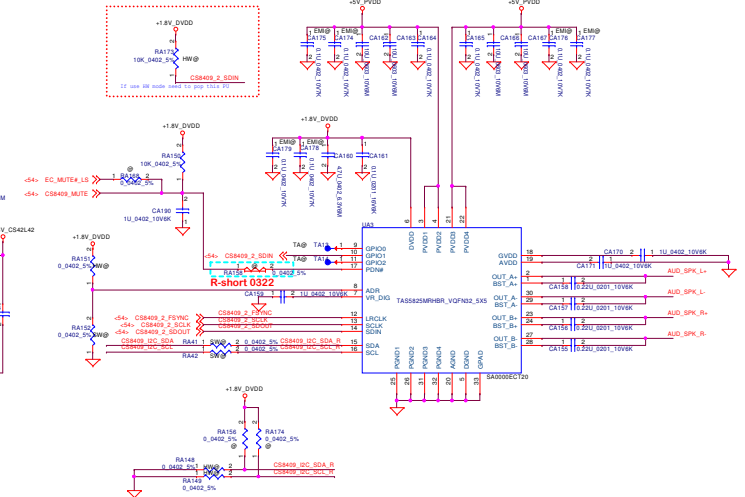
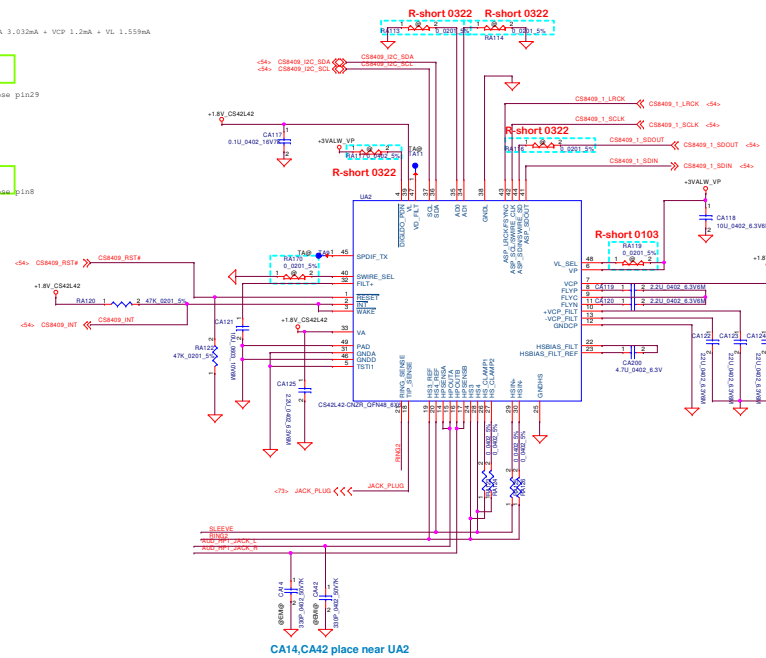
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**Universal Jack
(Use Global Headset Jack)**

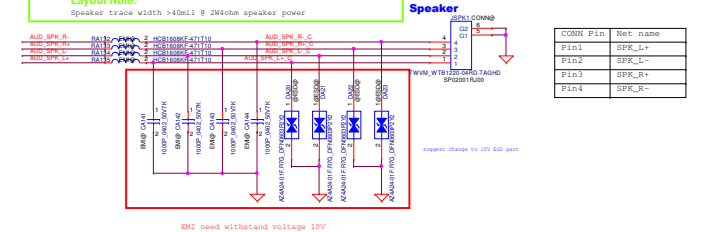


CS42142 Power state

1. Off configuration: Clock/data lines held low;
RESET = LOW; VA = VL = VCP = 0 V; VP = 3.6 V.
2. Standby configuration: Clock/data lines held low;
VA = VL = VCP = 0 V; VP = 3.6 V; M_MIC_WAKE = 0, M_HP_WAKE = 0 (unmasked).
3. Standby configuration (RCO clocking): Clock/data lines held low;
VA = 0 V; VL = 1.8 V, VCP = 0 V; VP = 3.6 V; M_MIC_WAKE = 0, M_HP_WAKE = 0 (unmasked).



Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power



CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R+
Pin4	SPK_R-

Reserve

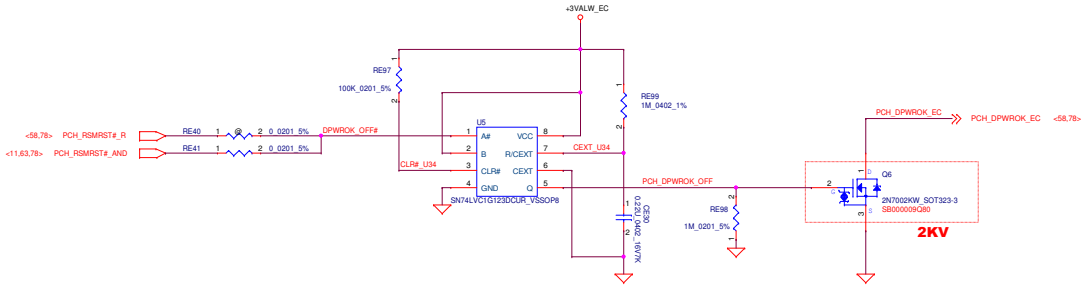
Reserve

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Main Function: WDT circuit

FUNCTION TABLE

INPUTS			OUTPUTS
CLR	\bar{A}	B	Q
L	X	X	L
X	H	X	L ⁽¹⁾
X	X	L	L ⁽¹⁾
H	L	\uparrow	\square
H	\downarrow	H	\square
\uparrow	L	H	\square



$t_{OUT}^{(2)}$	Q	$C_{out} = 28 \text{ pF}$ $R_{out} = 2 \text{ k}\Omega$	225	600	190	220	170	200	150	180	ns
		$C_{out} = 0.01 \text{ }\mu\text{F}$ $R_{out} = 10 \text{ k}\Omega$	100	110	100	110	100	110	100	110	μs
		$C_{out} = 0.1 \text{ }\mu\text{F}$ $R_{out} = 10 \text{ k}\Omega$	1	1.1	1	1.1	1	1.1	1	1.1	ms

Main Function: S5 LID

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General Specification	4.1. General Specifications			
	Item	Spec	Notes	
	System	Self-Contained type		
	Multi-Turn Transmits	100 points		
	Address range	Start to 0255		
	Turns	Type		
	Encoder	Advanced IC Teach Sensor (Contact PNP) IC	0.30mm (2 to 5.50mm(V) M2-4(3)	
	Teach IC information	IC	20 to 30	Unique
		(Base Address)	0x15	
		(P0)	0010	
		(P1)	0011	
		(P2)	0010	
	Number of Sensor Channel	4 (Base IC) x 3 (Max IC)		
	Interface	HEI meter (C)		

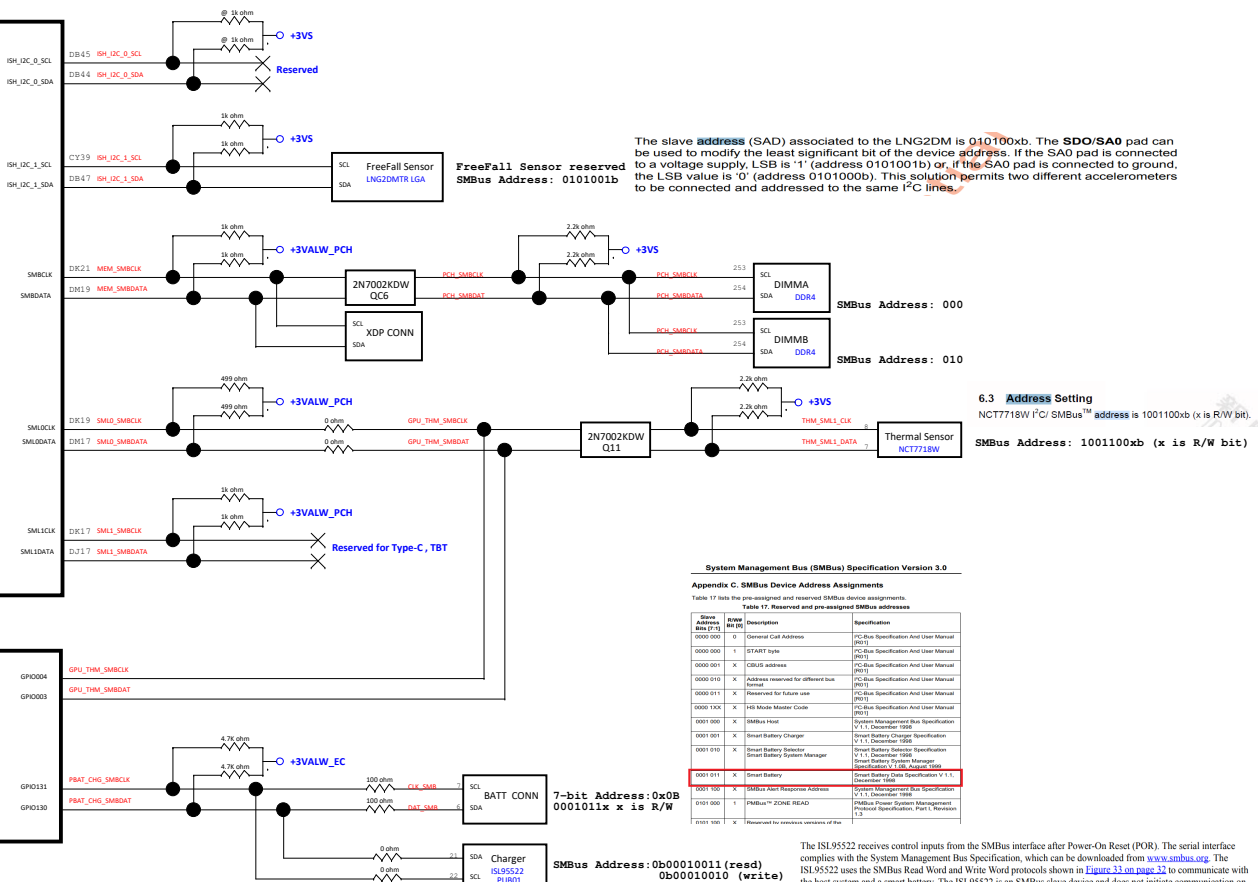
JeDP CONN
For Touch Screen

JTP CONN
Touch PAD
I2C

■ I²C
The I²C interface complies with I²C Bus Specification, Version 2.1.
The device address is 0x2C.
I²C clock rate: 400KHz

TGL-U

KBC
MEC 1515



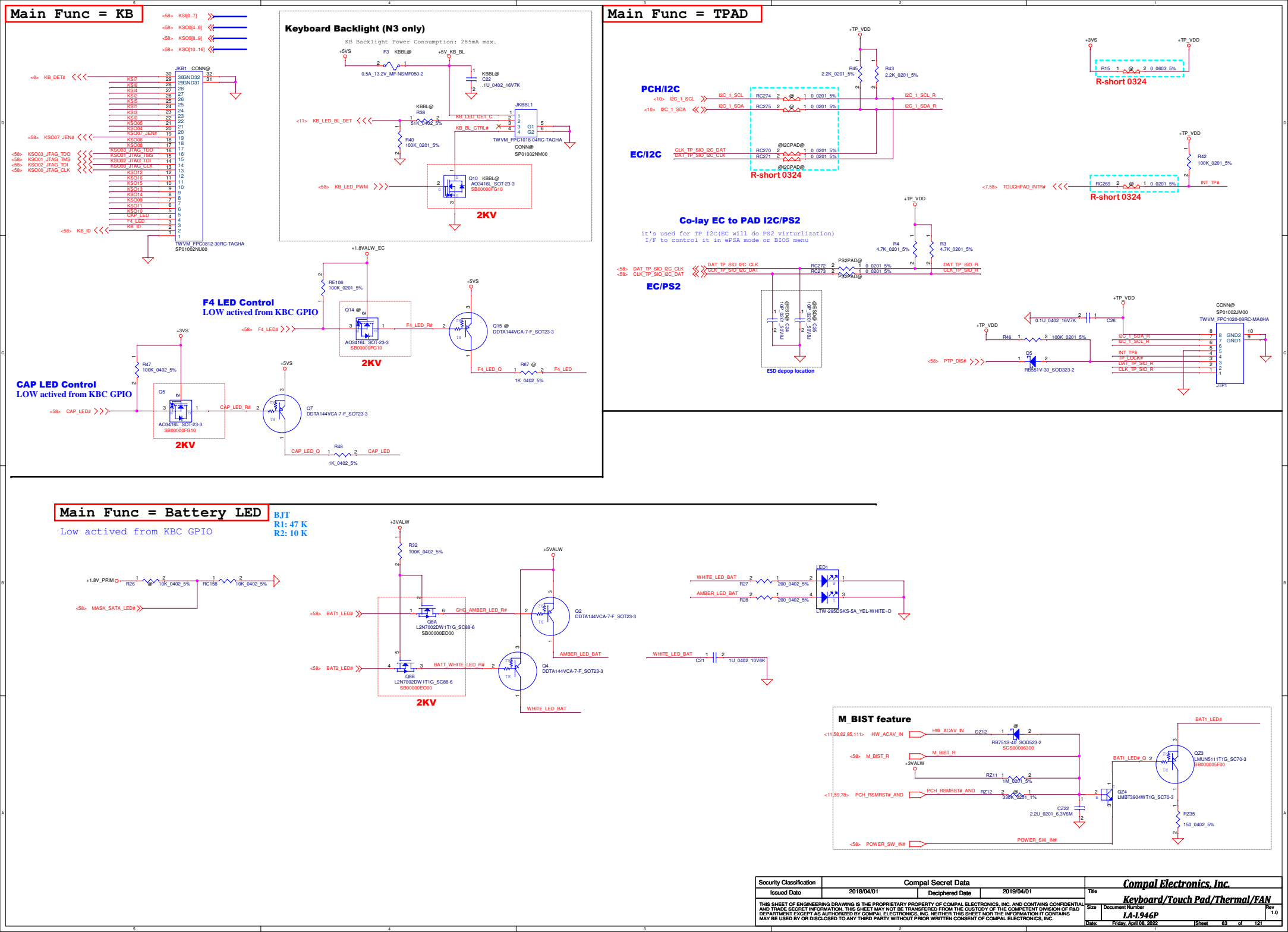
The ISL95522 receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification, which can be found on www.smbus.org. The ISL95522 uses the SMBus Read Word and Write Word protocols shown in [Figure 33 on page 32](#) to communicate with the host system and a smart battery. The ISL95522 is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001.

Read address = 0b0001001(0X13H)
Write address = 0b0001001(0X12H)

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				FLA-1596P		
				Date	Friday, April 6, 2012	Sheet 61 of 121

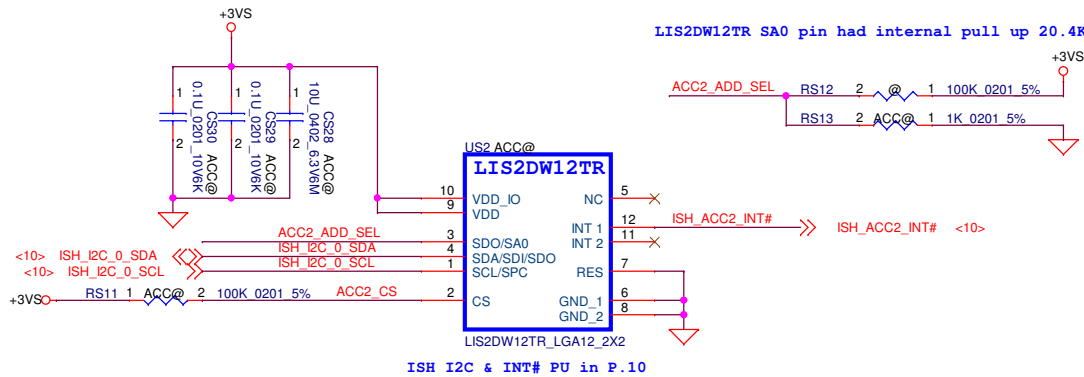
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Main Function: ACC sensor

Accelerometer-16bit



Reserve

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[illegible]

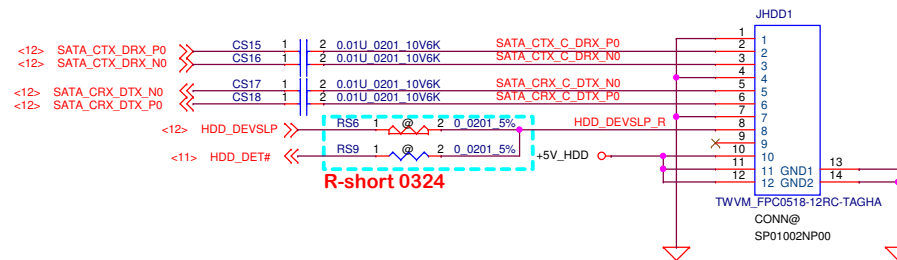
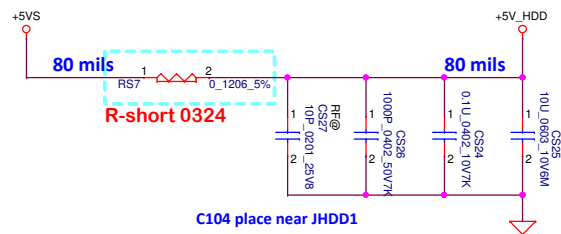
TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

[illegible]

The diagram illustrates the RTC power gating circuit. It features two main power rails: **RTC_SDC** and **RTC_CELL**, both labeled **2KV**. The **RTC_CELL** rail is connected to a MOSFET **Q17** (SB000015N00) through a resistor **R1** (1M_0402_5%). The **RTC_SDC** rail is connected to a MOSFET **Q16** (BD135) through a resistor **R2** (10K_0402_5%). The **RTCRST_ON** signal is connected to a MOSFET **Q18** (A03419L_SOT23-3) through a resistor **R3** (10K_0402_5%). The **RTCRST_ON** signal is also connected to a MOSFET **Q17** (SB000015N00) through a resistor **R4** (1M_0402_5%). The **RTCRST_ON** signal is also connected to a MOSFET **Q16** (BD135) through a resistor **R5** (100K_0402_5%). The **RTCRST_ON** signal is also connected to a MOSFET **Q18** (A03419L_SOT23-3) through a resistor **R6** (22K_0402_5%). The **RTCRST_ON** signal is also connected to a MOSFET **Q17** (SB000015N00) through a resistor **R1** (1M_0402_5%). The **RTCRST_ON** signal is also connected to a MOSFET **Q16** (BD135) through a resistor **R2** (10K_0402_5%). The **RTCRST_ON** signal is also connected to a MOSFET **Q18** (A03419L_SOT23-3) through a resistor **R3** (10K_0402_5%). The **RTCRST_ON** signal is also connected to a MOSFET **Q17** (SB000015N00) through a resistor **R4** (1M_0402_5%). The **RTCRST_ON** signal is also connected to a MOSFET **Q16** (BD135) through a resistor **R5** (100K_0402_5%). The **RTCRST_ON** signal is also connected to a MOSFET **Q18** (A03419L_SOT23-3) through a resistor **R6** (22K_0402_5%).

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				LA-19462				1.0
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Main Func = HDD&FFS



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	8
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	9

Main Func = ODD

Cancel ODD

Main Func = SSD M Key CONN

NGFF Key M

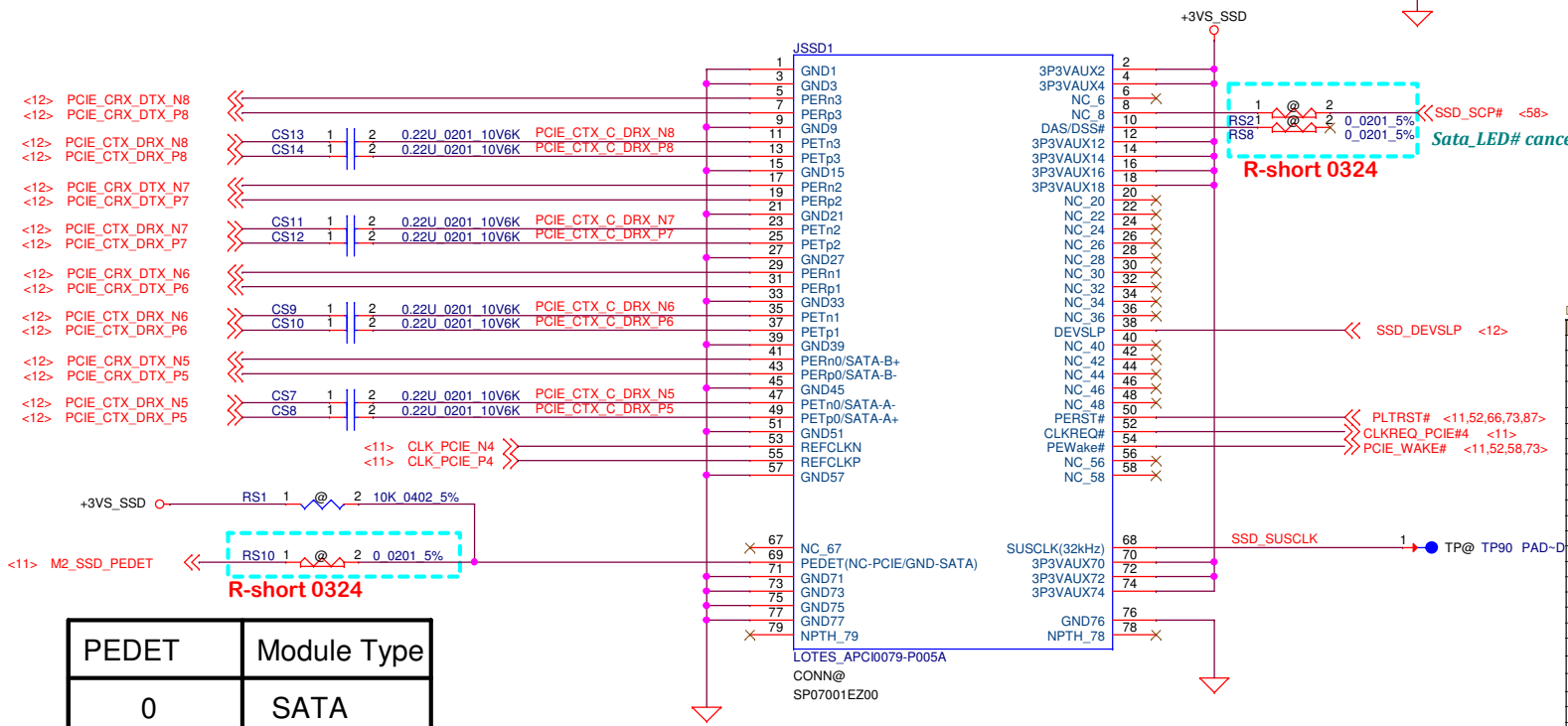


Table 11) Signal Assignments

Pin#	Assignment	Description	Pin#	Assignment	Description
1	GND	Return current path	2	3.3V	3.3V source
3	GND	Return current path	4	3.3V	3.3V source
5	PETn3	PCIe TX	6	NIC	NIC
7	PETp3	PCIe TX	8	PLP_INIT# (optional)	PLP Control Signal
9	GND	Return current path	10	LED#	Device Active Signal (Refer to Table 12)
11	PERn3	PCIe Rx	12	3.3V	3.3V source
13	PERp3	PCIe Rx	14	3.3V	3.3V source
15	GND	Return current path	16	3.3V	3.3V source
17	PETn2	PCIe TX	18	3.3V	3.3V source
19	PETp2	PCIe TX	20	NIC	NIC
21	GND	Return current path	22	NIC	NIC
23	PERn2	PCIe Rx	24	NIC	NIC
25	PERp2	PCIe Rx	26	NIC	NIC
27	GND	Return current path	28	NIC	NIC
29	PETn1	PCIe TX	30	NIC	NIC
31	PETp1	PCIe TX	32	NIC	NIC
33	GND	Return current path	34	NIC	NIC
35	PERn1	PCIe Rx	36	NIC	NIC
37	PERp1	PCIe Rx	38	NIC	NIC
39	GND	Return current path	40	SMB_CLK (I/O) ²	DMU (Do Not Use)
41	PETn0	PCIe TX	42	SMB_DATA (I/O) ²	DMU (Do Not Use)
43	PETp0	PCIe TX	44	ALERT# (I/O) ¹	DMU (Do Not Use)
45	GND	Return current path	46	NIC	NIC
47	PERn0	PCIe Rx	48	NIC	NIC
49	PERp0	PCIe Rx	50	PENST#	PCIe Reset
51	GND	Return current path	52	CLKREQ#	PCIe Device Clock Request
53	REFCLKN	PCIe Reference Clock	54	PEWake#	NIC
55	REFCLKP	PCIe Reference Clock	56	Reserved for MFG., Data	DMU (Do Not Use)
57	GND	Return current path	58	Reserved for MFG., Clock	DMU (Do Not Use)
67	NIC	NIC	68	SUSCLK	DMU (Do Not Use)
69	PEDET	NIC	70	3.3V	3.3V source
71	GND	Return current path	72	3.3V	3.3V source
73	GND	Return current path	74	3.3V	3.3V source
75	GND	Return current path	76	3.3V	3.3V source
77	GND	Return current path	78	3.3V	3.3V source
79	GND	Return current path	80	3.3V	3.3V source

PEDET	Module Type
0	SATA
1	PCIE

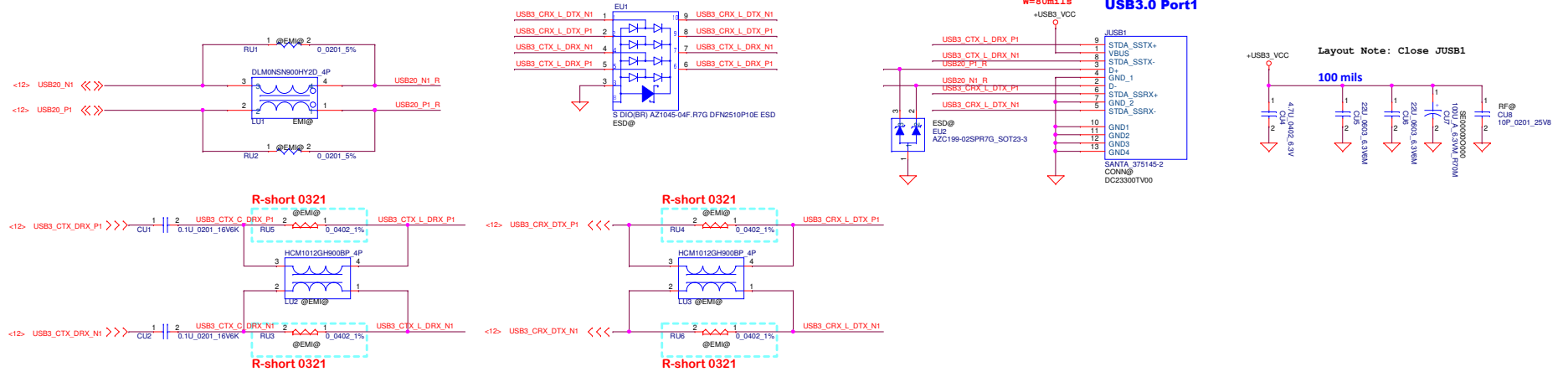
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				Sheet 69 of 121	

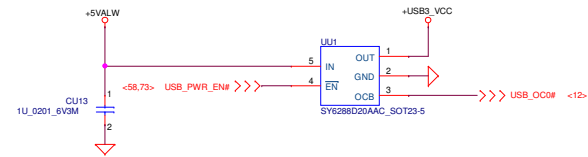
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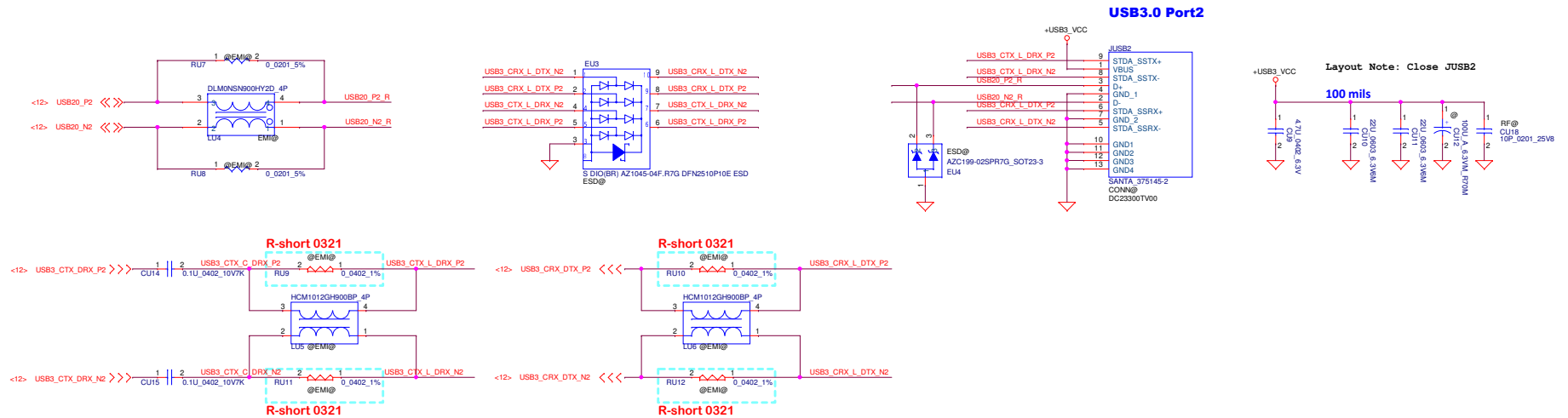
Main Func = USB3.0 Port1



Maximum Output
Current 2A



Main Func = USB3.0 Port2

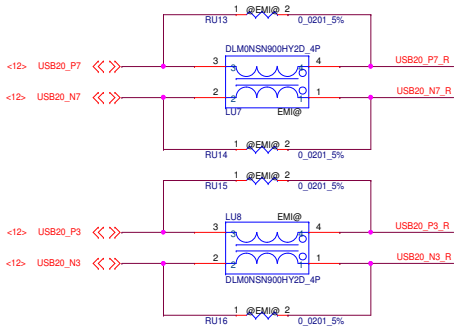
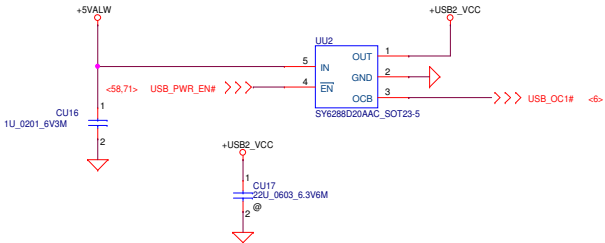


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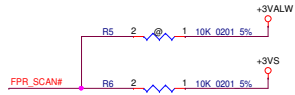
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					LA-L946P	1.0
				Date:	Friday, April 08, 2022	Sheet 72 of 121

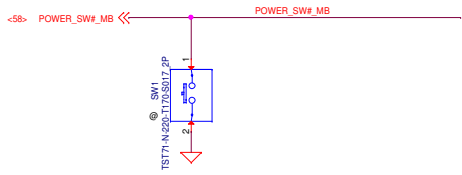
Main Func = USB2.0 Port3 + Card Reader on IO/B



Main Func = FPR

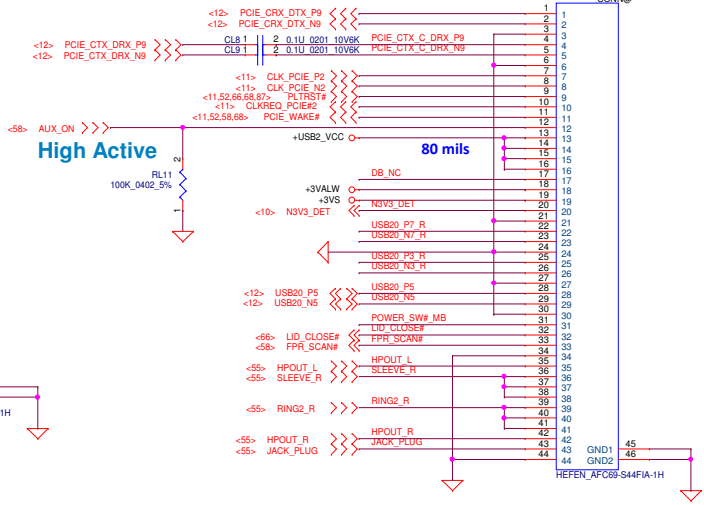
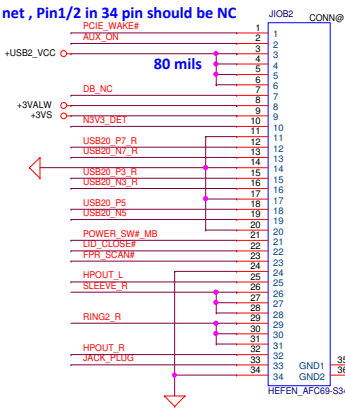


Main Func = PWR Button



JIOB1 and JIOB2 CONN co-lay

for co-lay add net, Pin1/2 in 34 pin should be NC



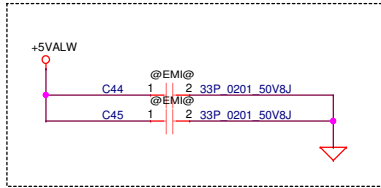
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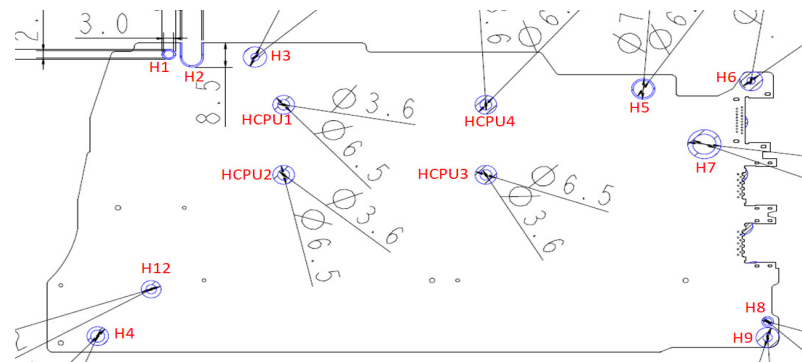
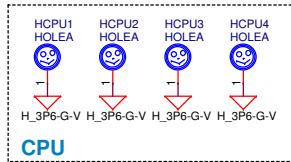
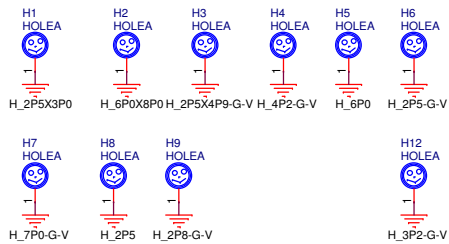
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EMI reserve bridge

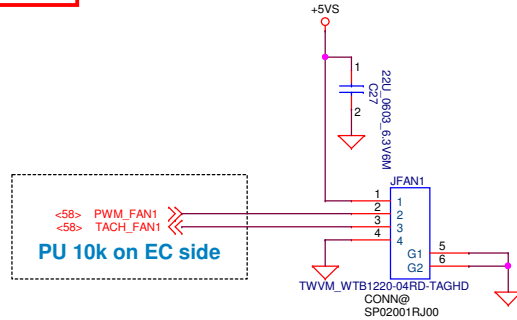


Screw hole/FD



1029 ME update

FAN

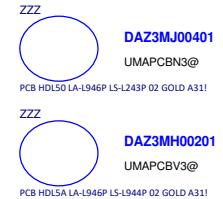


PU 10k on EC side

need to check pin define with Thermal

PCB PN

PCB R3 DAZ



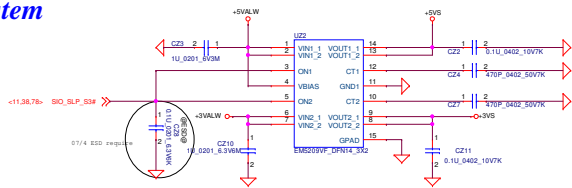
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Date: Friday, April 08, 2022				Sheet 77 of 121

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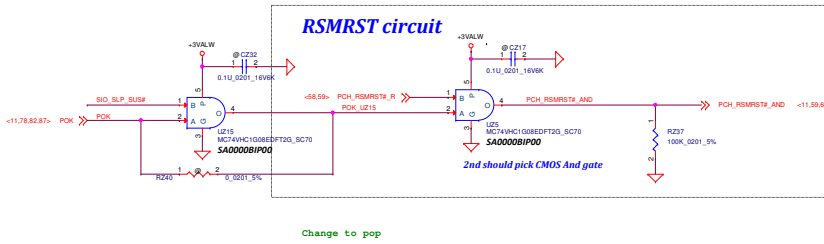
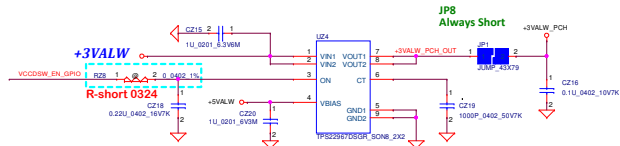
PWRBTN/PCB PN//SCREW/FAN

LA-L946P

+5VS / +3VS for System

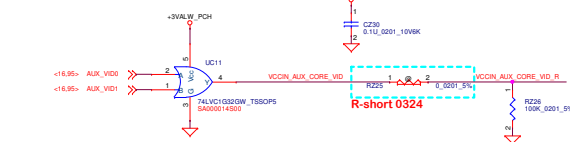
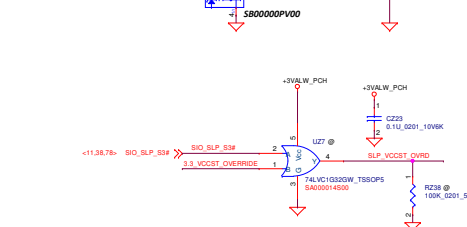
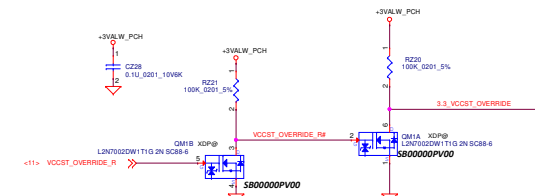


+3VALW TO +3VALW_PCH



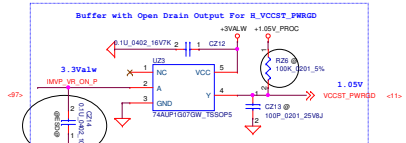
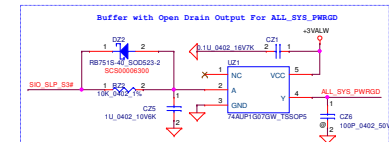
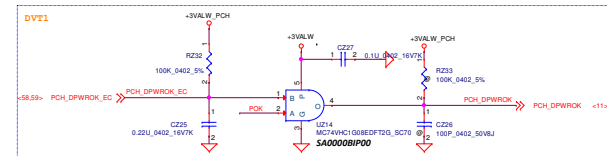
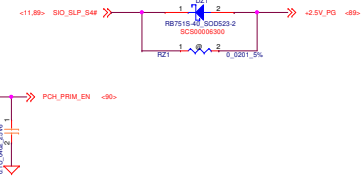
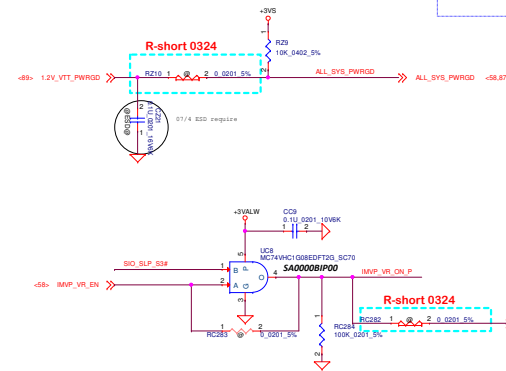
1.05V_PROC

VCCST_OVERRIDE_R# VCCST_OVERRIDE_R# <79>



Sequence Logic

IMVP_VR_ON&VCCST_PWRGD

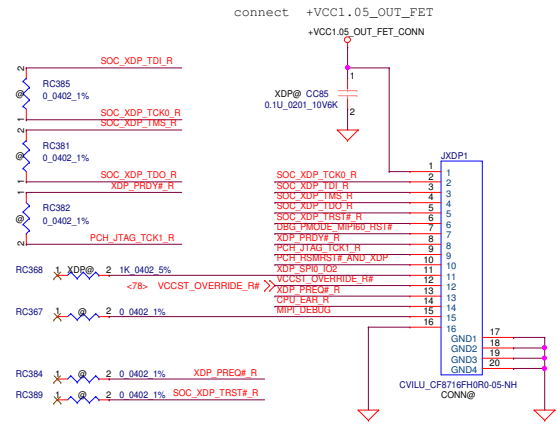


SN74AUP1CFUNCTION TABLE

C		A		B		Y	
L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L
L	L	L	L	H	L	L	L
L	L	L	H	H	L	L	L
L	L	L	L	L	H	L	L
L	L	L	H	L	H	L	L
L	L	L	H	H	L	L	L
L	L	L	H	H	H	L	L
L	L	L	L	L	L	H	L
L	L	L	L	L	H	L	L
L	L	L	L	H	L	L	L
L	L	L	L	H	H	L	L
L	L	L	L	H	H	H	L
L	L	L	L	H	H	H	H

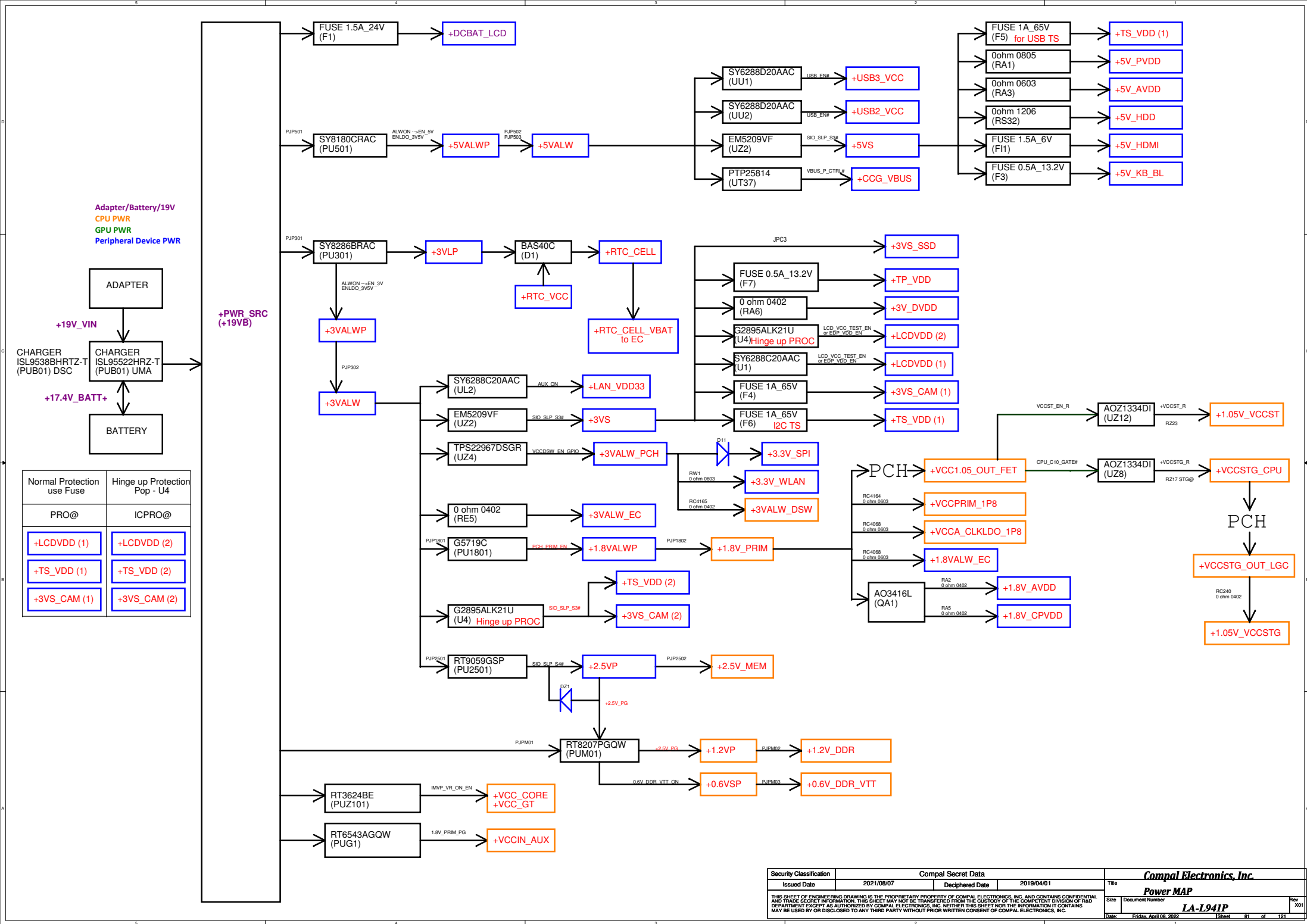
Main Func = Debug connector

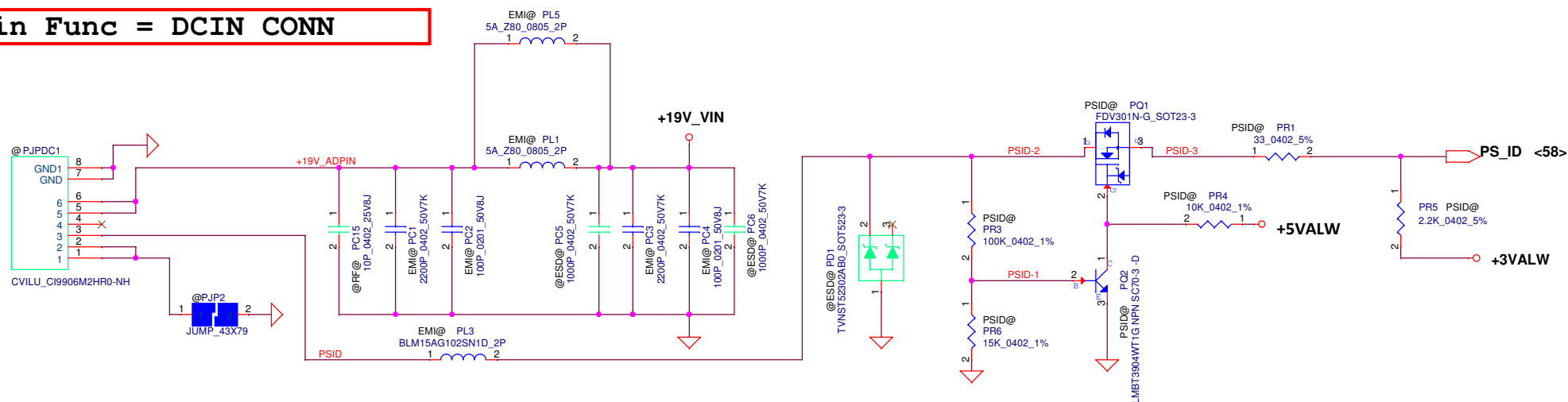
connect PLTRST# to RC369 pin1
connect DBG_PMODE to RC369 pin2
RC369 1 2 1K 0201 5% DBG_PMODE_MIP60_RST#
RC370 1 XDP# 2 1K 0201 5% PCH_RSMRST#_AND_XDP
connect PCH_RSMRST#_AND to RC370



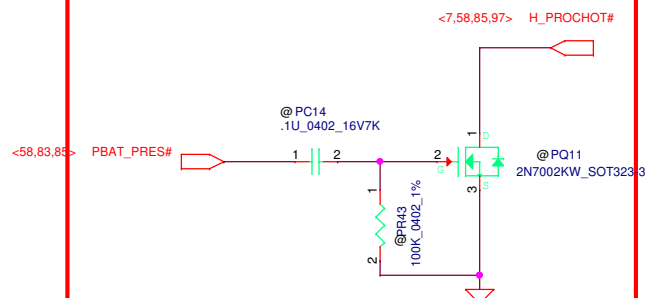
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				Document Number	LA-L946P
				Date:	Friday, April 08, 2022
				Sheet	80 of 121

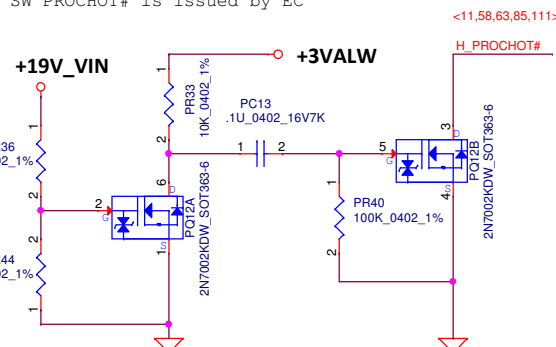
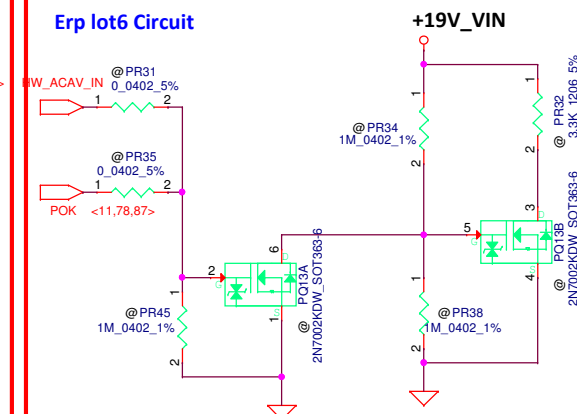


**Adapter protection:**

if battery removed, adaptor only, then trigger the H_PROCHOT#, keep @ in BOM since battery can not be removed by end user

**Battery protection:**

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC

**Erp lot6 Circuit**

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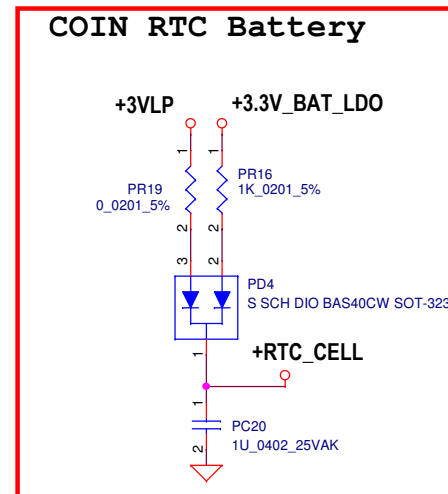
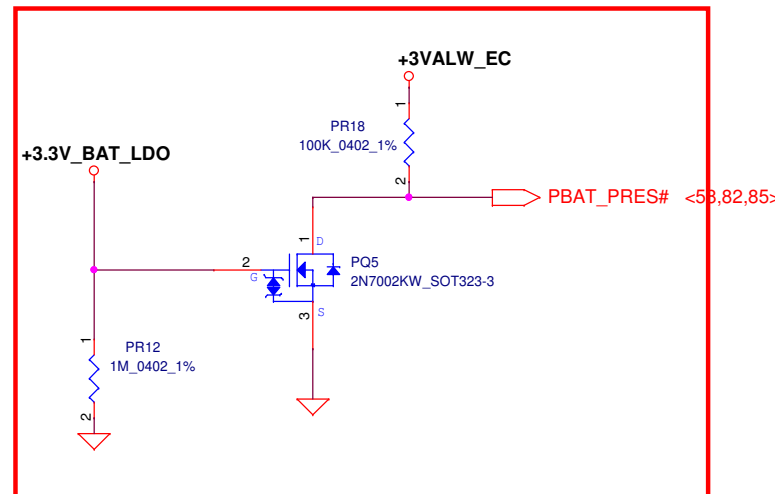
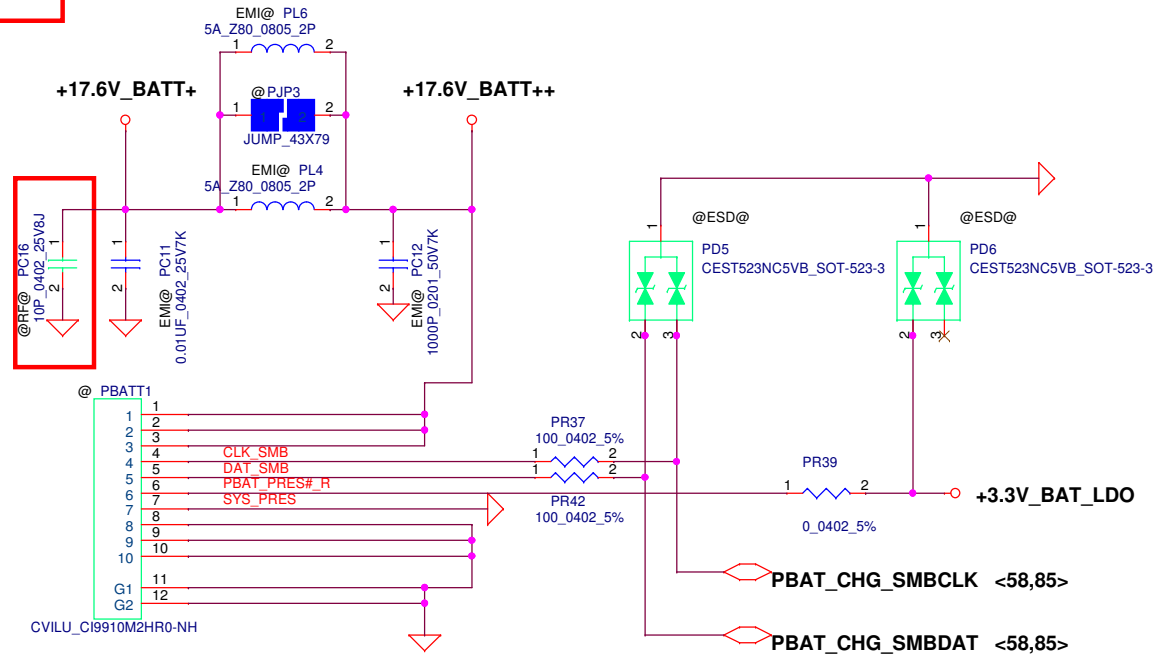
PWR DCIN CONN

Rev X01

Battery Bot Side

PIN1 GND
 PIN2 GND
 PIN3 GND
 PIN4 SYS_PRES
 PIN5 BATT_PRS
 PIN6 DAT_SMB
 PIN7 CLK_SMB
 PIN8 Batt+
 PIN9 Batt+
 PIN10 Batt+
 SP021412220

ACES_50458-01001-P01_10P-T



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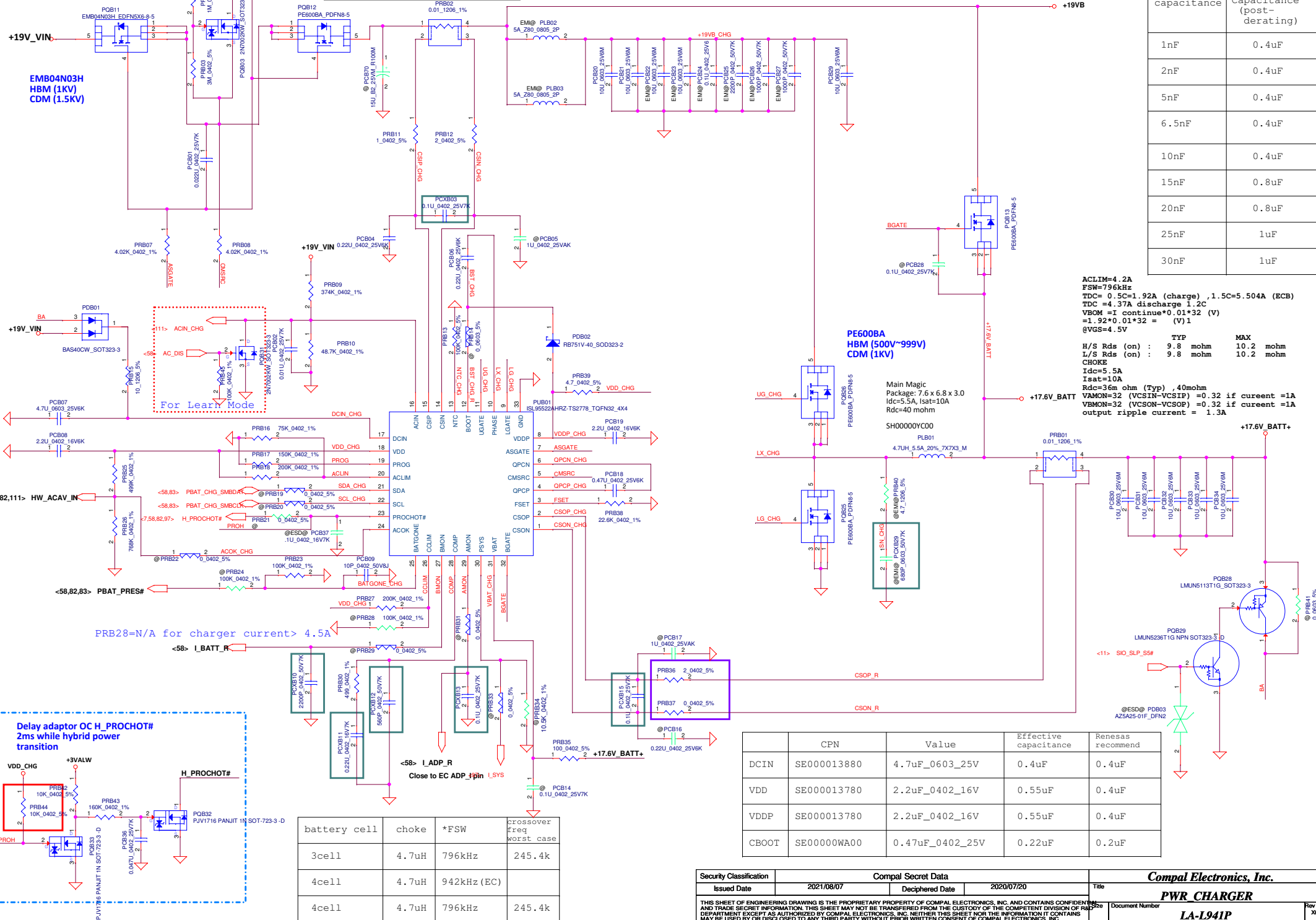
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Date: Friday, April 08, 2022		Sheet 83 of 121		Rev X01	

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				Size	Document Number
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Main Func = CHARGER

65W adaptor
Input ripple current : 0.65A



Lgate capacitance	Effective LDO output Capacitance (post-derating)
1nF	0.4uF
2nF	0.4uF
5nF	0.4uF
6.5nF	0.4uF
10nF	0.4uF
15nF	0.8uF
20nF	0.8uF
25nF	1uF
30nF	1uF

```

ACLI=4.2A
FSW=756kHz
TDC= -0.192A (charge) , 1.5C=5.474A (ECB)
TDC = -3.07A discharge 1.2C
VBM = I= current*0.01+32 (V)
= 1.92*0.01+32 = (V1)
@VGS4.5V

                                TYP      MAX
H/S Rds (on) :      9.8  mohm      10.2  mohm
L/S Rds (on) :      9.8  mohm      10.2  mohm
CHOKE
Idc=5.5A
Isat=10A
Rds-36m ohm (Typ) 40mohm
VVMON=32 (VCSIN-VCSIP) = 0.32 if current=1A
VBMON=32 (VCSON-VCSOP) =0.32 if current=1A
output ripple current = 1.3A

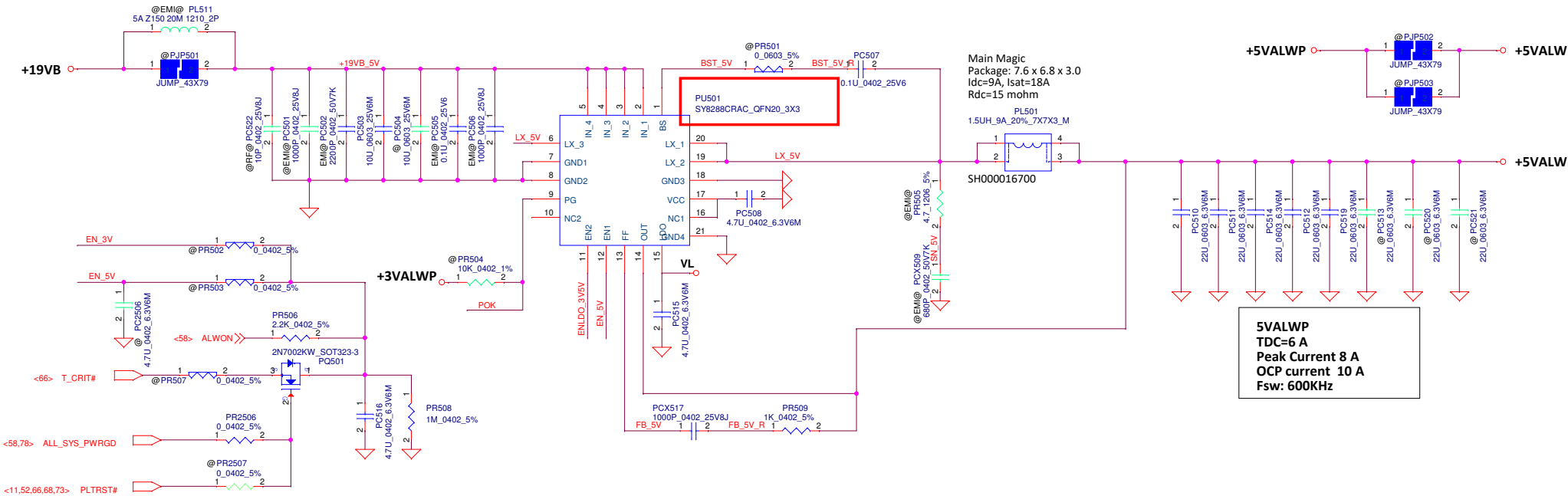
```

	CPN	Value	Effective capacitance	Renesas recommend
DCIN	SE000013880	4.7uF_0603_25V	0.4uF	0.4uF
VDD	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
VDDP	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
CBOOT	SE00000WA00	0.47uF_0402_25V	0.22uF	0.2uF

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					LA-L941P Date: Friday, April 06, 2022
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				Size	Document Number
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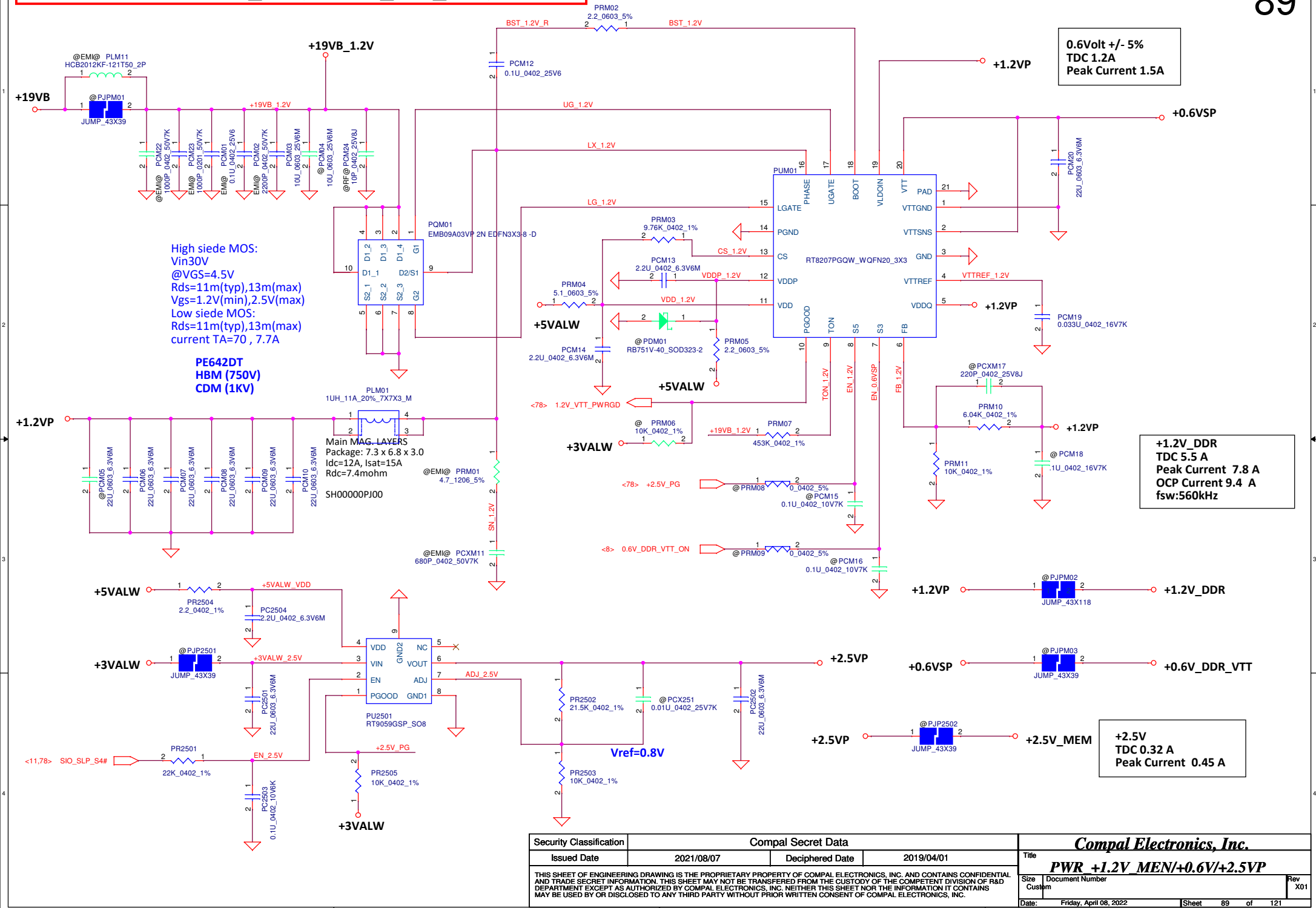


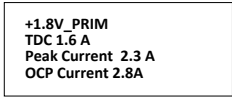
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Issued Date	2021/08/07	Deciphered Date	2019/04/01	Title	PWR 3.3VALWP/SVALWP	
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				Date:	Fri Aug 06 2022	ISheet

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				Size	Document Number
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Main Func = +1.2V_DDR/+0.6V_DDR_VTT/ +2.5VP





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Date:	Friday, April 08, 2022		Sheet	90	of	121

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				Size	Document Number	Rev
				Date: Friday, April 08, 2022		Sheet 91 of 121

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ADL-P_15W
+VCCIN_AUX
TDC=14A
ICCMAX=32A
OCP=38.4A
DC LL=2.0m ohm
AC LL=3.4m ohm
Fsw: 600KHz

OCP is Lowside MOSFET Rdson sense

20210408 Modify for
Richtek review

+5VALW

+3VALW

+5VALW

5V: 800KHz
Float: 600KHz
GND: 400KHz

+19VB_AUX

20210408 Modify for
Richtek review

+19VB_AUX

+19VB

+VCCIN_AUX

Main MAG. LAYERS
Package: 7.3 x 6.8 x 3
Idc=35A, Isat=50A
Rdc=0.85 mohm
SH000012500

7*7*3
Rdc:0.85m+/-5%
Idc:35A
Isat:50A

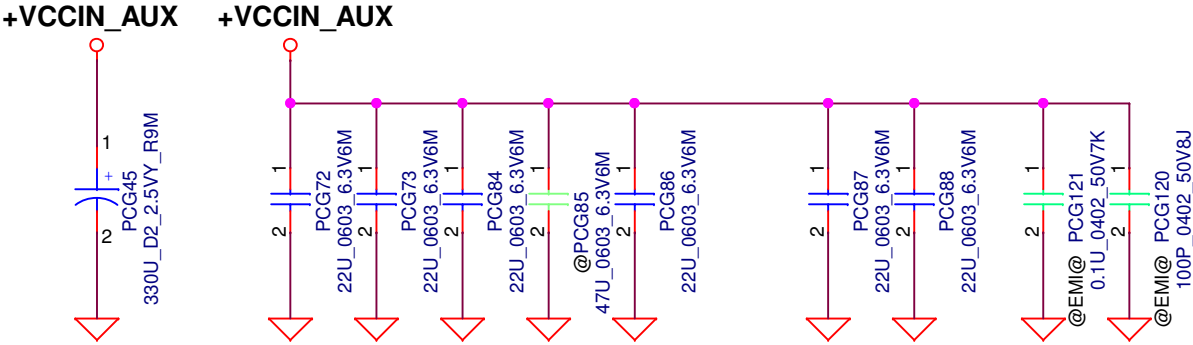
20210408 Modify for
Richtek review

+VCCIN_AUX

VCCIN_AUX VID Follow Intel PDG Rev0.71

VID1	VID0	+VCCIN_AUX Voltage
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

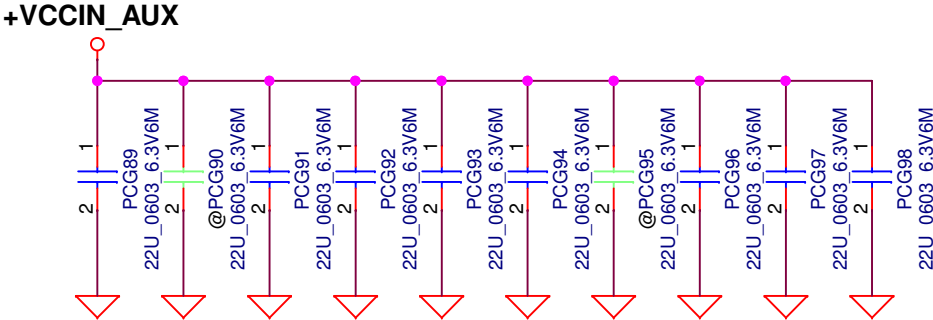
Main Func = VCCIN_AUX Decoupling



ADL-P_15W

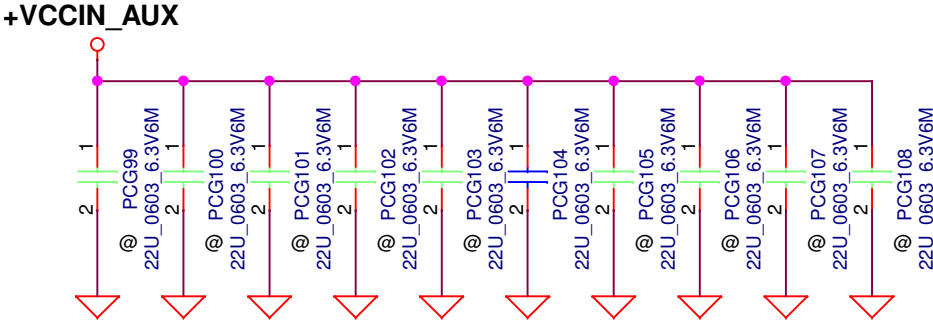
+VCCIN_AUX

ICCMAX=32A
TDC=14A
OCP=38.4A
DC LL=2.0m ohm
AC LL=3.4m ohm

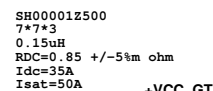
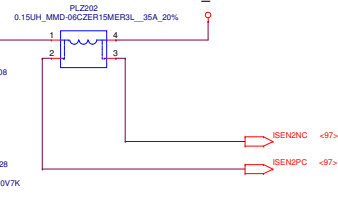
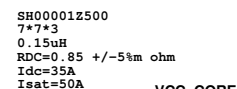
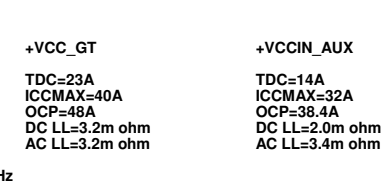


+VCCIN_AUX O/P caps:

330U_D2_2.5VM_R9M * 1pcs
22U/6.3V/X5R/0603 * 15 pcs



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				Size	Document Number	Rev X01
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				Date Friday, April 08, 2022	LA-1941P [Signal]
				98	151

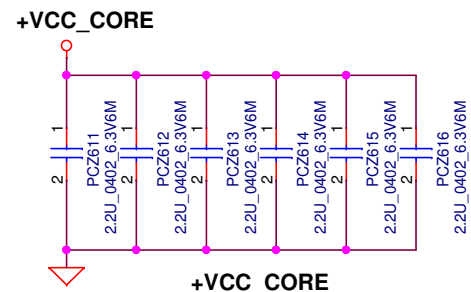
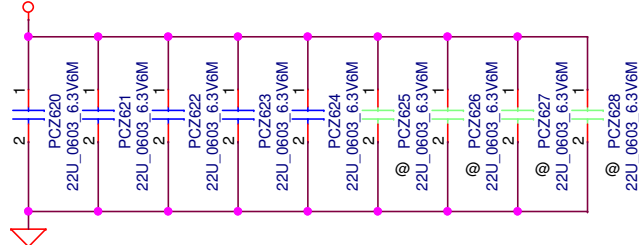
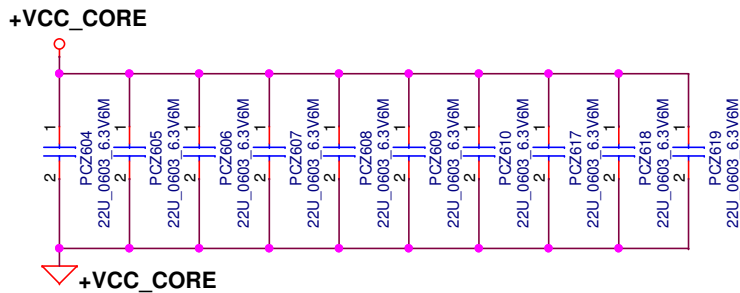
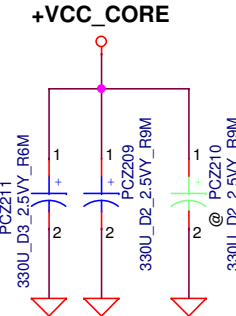
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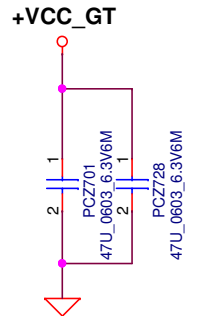
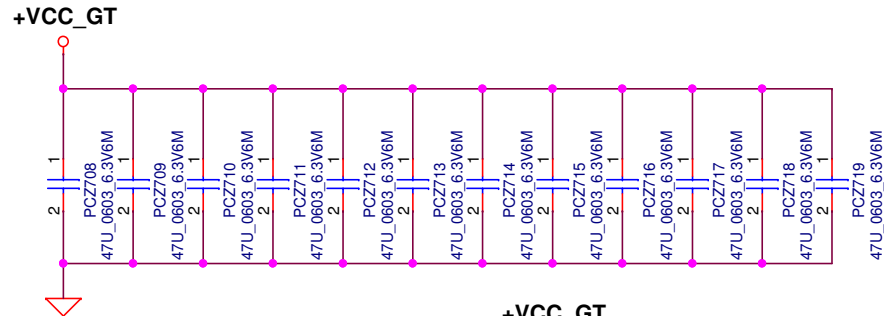
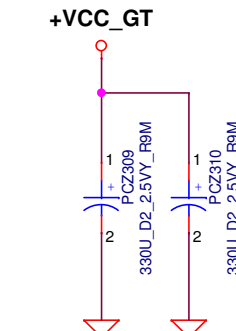
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Main Func = VCCIN Decoupling



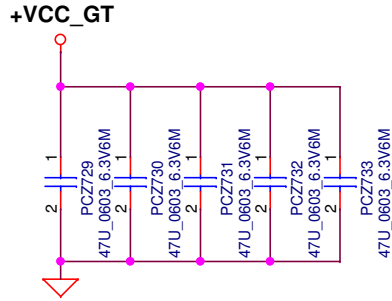
+VCC_CORE O/P caps:

- 330U_D2_2.5VM_R9M * 1pcs
- 330U_D3_2.5VY_R6M* 1pcs
- 47U/6.3V/X5R/0603 * 3 pcs
- 2.2U/6.3V/X5R/0402 * 6 pcs
- 22U/6.3V/X5R/0603 * 14 pcs



+VCC_GT O/P caps:

- 330U_D2_2.5VM_R9M * 2pcs
- 47U/6.3V/X5R/0603 * 17 pcs



Function feild:
+VCC_CORE output cap:36.4
+VCC_GT output cap:36.5

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P87	3.3/5VALWP	20210709	COMPAL	Thermal design SIF/ARK have encountered OTP problems	ALL_SYS_PWRGD Trace add PR2506 0_0402_5% PQ501 Pin 2 add PLTRST# and PR2507 0_0402_5% parallel ALL_SYS_PWRGD	0.1
2	P95	VCCIN_AUX	20210709	COMPAL	Net name overlapping	Modify ISENSEN_RT6543_R net name	0.1
3	P97	VCCIN_AUX	20210712	COMPAL	Change common part and COS issue	change PHZ101,PHZ102 form SL200000V00 to SL200002H00 (common part) change PHZ103,PHZ104,PHZ105 from SL200000W00 to SL200002F00 (common part) change PCZ102 from SE00001ERM0 to SE00000WA00 for COS issue change PCXZ09 from SE000014700 to SE071820J80 for COS issue change PCZ130 from SE124224K80 to SE000015W00 for COS issue	0.1
4	P97	VCCIN/GT	20210730	COMPAL	Richtek VRTT test recommend	PRZ135,PRZ138 change from 5.23k to 5.36k ohm for LL PRZ104 change from 332k to 240k ohm for FRQ-Core	0.1
5	P95-97	VCCIN-VCCIN/GT	20210730	COMPAL	Richtek VRTT test recommend	PRZ152 change from 15Kohm to 10Kohm for DVID PRZ151 change from 53.6k to 36Kohm for DVID PCG13 change 390pF to 100pF for COMP-AUX PRG24 change 1.6kohm to 1ohm for COMP-AUX PCG16=NC for COMP-AUX	0.1
6	P101	+VCORE	20210730	COMPAL	Richtek VRTT test recommend	Remove PCZ210,Put on PCZ211	0.1
7	P101	VCCGT	20210730	COMPAL	Richtek VRTT test recommend	VCCGT: Core side put on the 47uF*17 (22uF change to 47uF) change list:PCZ708 PCZ709 PCZ710 PCZ711 PCZ712 PCZ713 PCZ714 PCZ715 PCZ716 PCZ717 PCZ718 PCZ719 PCZ729 PCZ730 PCZ731 PCZ732 PCZ733	0.1
8	P96	AUX	20210730	COMPAL	Richtek VRTT test recommend	PCB88,PCG87:change from 10uf to 22uF PCB72,PCB73,PCB84,PCB86:change from 47uf to 22uF PCG88, PCG93, PCG96, PCG94, PCG98, PCG97, PCG86, PCG84, PCG73, PCG72, PCG104, PCG87, PCG89, PCG92, PCG91 ,15 pcs 22uF other depop	0.1
9	P82	DC IN	20210802	COMPAL	ESD request	Remove PD2, PD3, PR7	0.1
10	P96	VCCIN_AUX Decoupling	20210802	COMPAL	EMI request for reserve	Add PCG120, 0.1u_0402, reserve for @EMI@ Add PCG121, 100p_0402, reserve for @EMI@	0.1
11	P97	VCCIN_GT	20210802	COMPAL	Intel recommend	PCG103 change to from 0.1u to 330pF, pop	0.1
12	P82	DCIN CONN_PW	20210803	COMPAL	EMI request	Remove P12	0.1
13	P87	3.3/5VALWP	20210803	COMPAL	HW request for thermal sensor control	pop PR2506,depop PR2507	0.1
14	P95 P97	VCCIN_AUX VCCIN_GT	20210804	COMPAL	Net name overlapping	Modify ISENSEN_AUX net name	0.1
						<div> <div>Security Classification</div> <div>Compal Secret Data</div> <div>Issued Date</div> <div>2021/08/07</div> <div>Deciphered Date</div> <div>2019/04/01</div> </div> <div> <div>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</div> <div> <div>Compal Electronics, Inc.</div> <div>Changed-List PWR History</div> <div> <div>Title</div> <div>Document Number</div> <div>Rev</div> <div>X01</div> </div> </div> </div>	

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15	98	VCCIN-SW	20210809	COMPAL	Acoustic request	PCZ131 change to depop	0.1
16	97	VCCIN/GT_PW	20211007	COMPAL	Richtek recommened	PRZ135 PRZ138 change form 5.36kohm to 4.99kohm	0.2
17	97	VCCIN/GT_PW	20211007	COMPAL	Richtek recommened	PCXZ12 change from 82pF to 68pF	0.2
18	101	+VCORE_PW	2021112	COMPAL	Cost down concern	PCZ603 change from 47uF to 22uF	0.2
19	101	+VCORE_PW	2021112	COMPAL	Cost down concern	PCZ624 change to pop	0.2
20	97	VCCIN/GT_PW	20220216	COMPAL	Richtek recommened, VRTT test result	PRZ148 change from 100ohm to 2.2nF	0.3
21	97	VCCIN/GT_PW	20220216	COMPAL	Richtek recommened, VRTT test result	PCZ108 change to pop 2.2nF	0.3
22	97	VCCIN/GT_PW	20220216	COMPAL	Richtek recommened, VRTT test result	PRZ143 PRZ147 change from 0ohm to 2.2ohm	0.3
23	85	CHARGER_PW	20220210	COMPAL	Shortpad request	PRB19 PRB20 PRB22 PRB29 PRB31 PRB33 PRB14 change to shortpad	0.3
24	87	3.3VALWP/ 5VALWP_PW	20220210	COMPAL	Shortpad request	PR301 PR501 PR502 PR503 PR507 change to shortpad	0.3
25	89	+1.2V_DDR/ +0.6V/ +2.5VP_PW	20220210	COMPAL	Shortpad request	PRM08 PRM09 change to shortpad	0.3
26	90	+1.8V_PW	20220210	COMPAL	Shortpad request	PR1801 change to shortpad	0.3
27	95	VCCIN_AUX_PW	20220210	COMPAL	Shortpad request	PRG6 PRG11 PRG30 PRG27 PRG17 PRG38 change to shortpad	0.3
28	97	VCCIN/GT_PW	20220210	COMPAL	Shortpad request	PRZ134 PRZ120 PRZ124 PRZ200 PRZ128 PRZ129 PRZ130 PRZ149 PRZ153 change to shortpad	0.3
29	98	VCCIN-SW_PW	20220210	COMPAL	Shortpad request	PRZ218 PRZ220 PRZ310 change to shortpad	0.3

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